

MODEL NAME : ZAL00
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WW000 LA-A491P M/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

2013-05-15 Rev: 0.3

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS VENUS : VENUS@,DIS@,EMI@,ESD@,RF@,XDP@



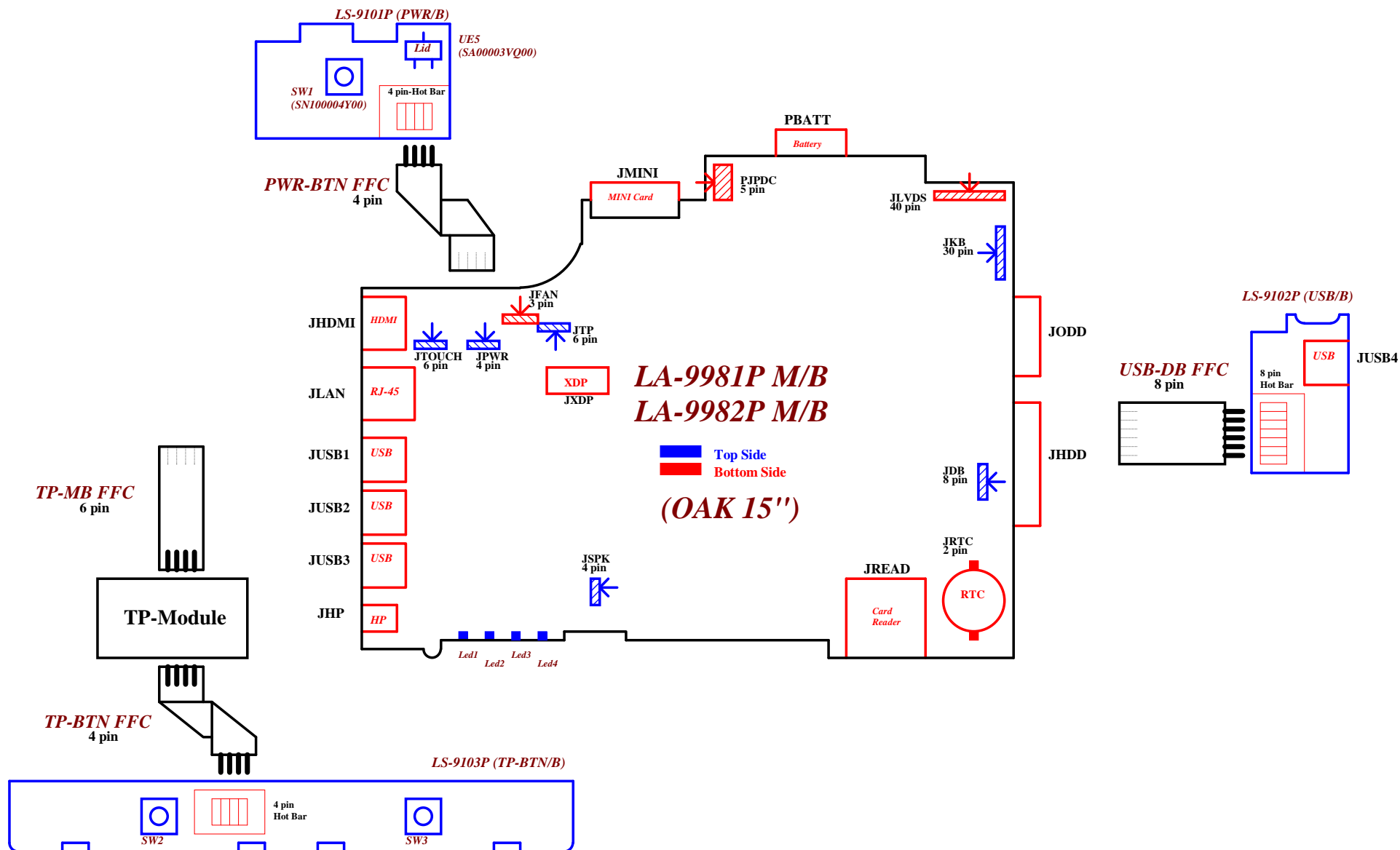
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Cover Page	
2013/04/01		2014/05/01		Document Number	
				LA-A491P	
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Project Code : VAW00 / VAW01

File Name : LA-9981P / LA-9982P



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Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	DB block diagram
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

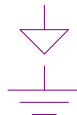
	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

BOARD ID Table

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0
16				

Symbol Note :



: means Digital Ground



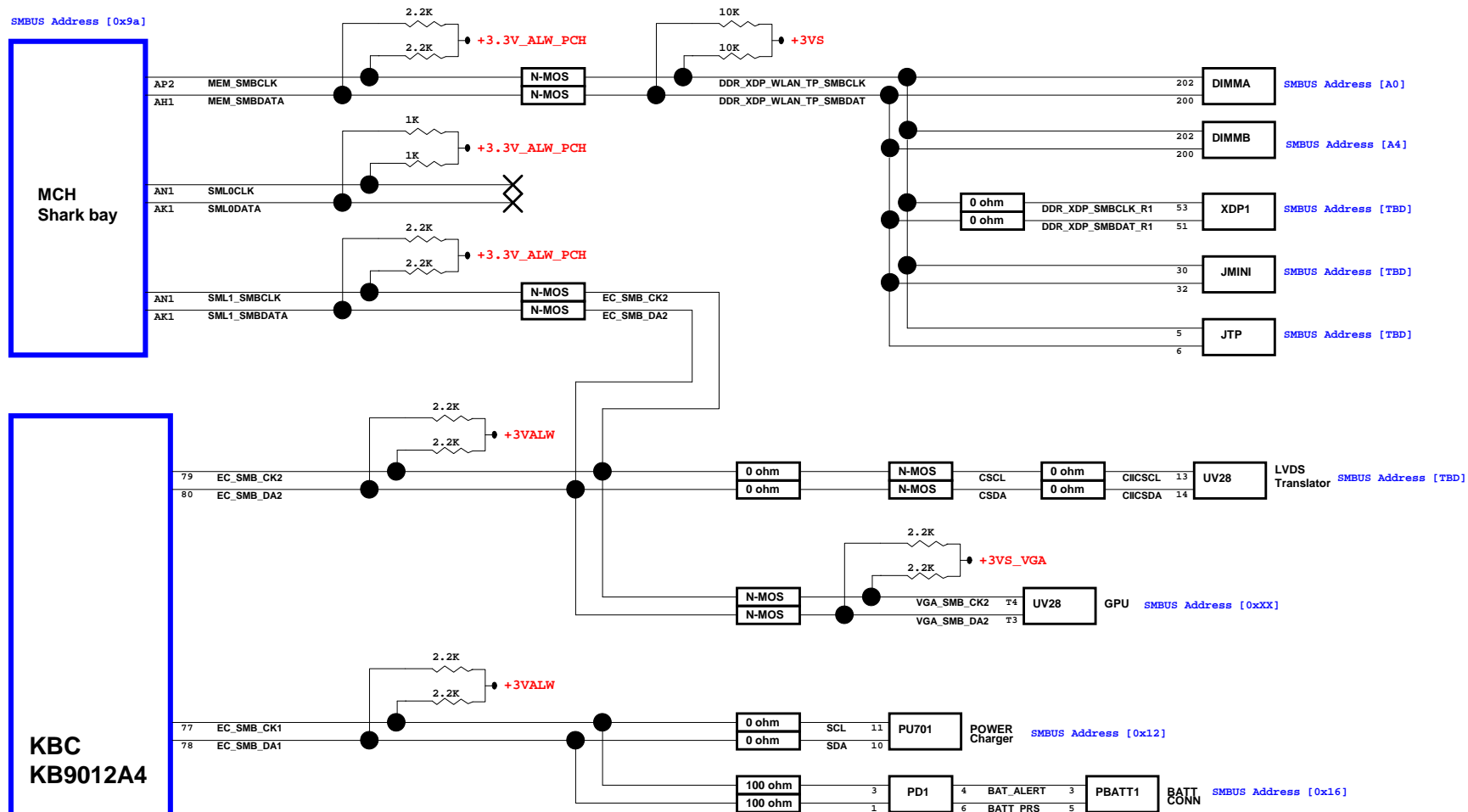
: means Analog Ground

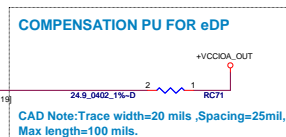
CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT

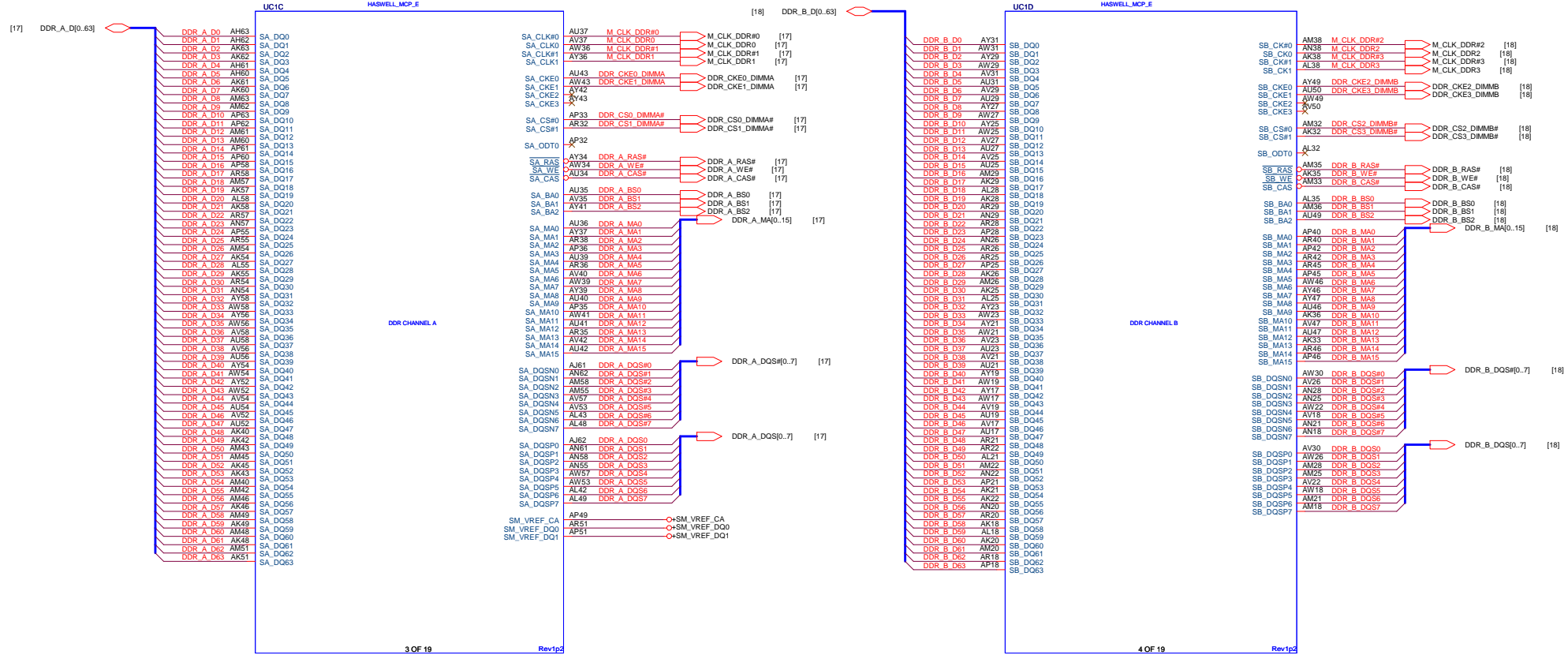
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

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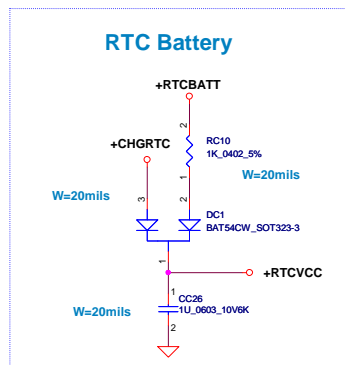


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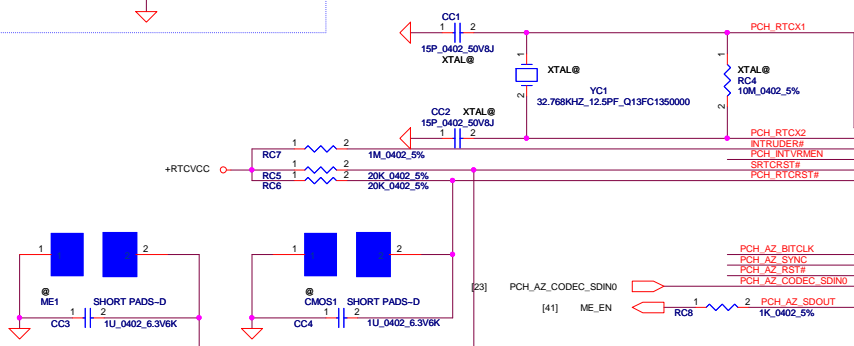


confirm by intel request PDG P141

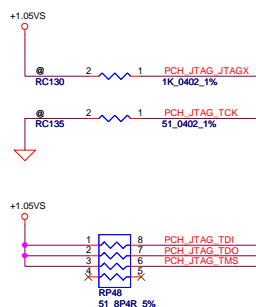
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Issued Date	2013/03/06	Deciphered Date	2014/04/01	MCP(3,4/19) DDR3	
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For GCLK

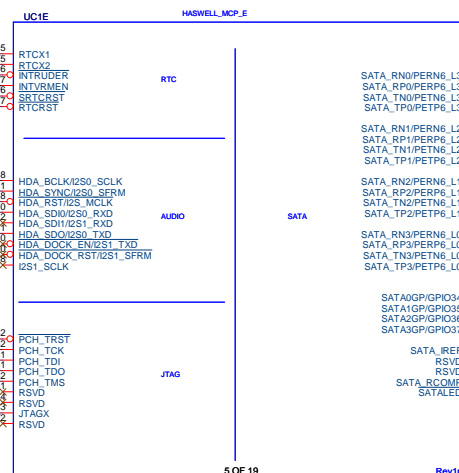


CMOS place near DIMM

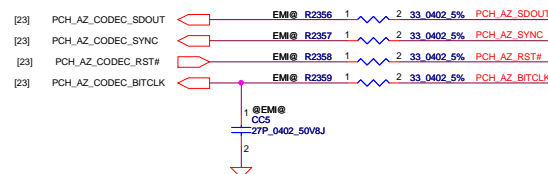


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

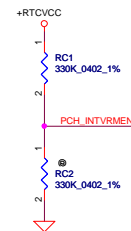
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



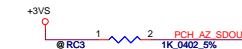
HDA for Codec



EMI depop location



INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED

PCH Rx side need use strap pin to update PCIE +/-

+3VS

RC107 10K_0402_5%

+1.05VS_ASATA3PLL

RC126 1 2 0.0603_1%

RC131 1 2 3.01K_0402_1%

SATA_ACT# [27]

within 500 mils

CAD note:

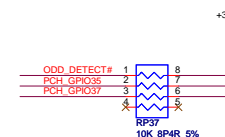
Place the resistor within 500 mils of the PCH. Avoid

routing next to clock pins.

reference FFRD sch 0.5

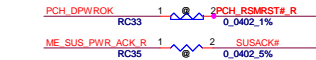
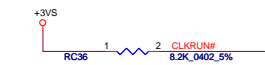
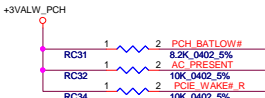
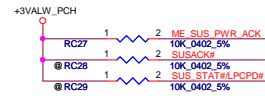
SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid
routing next to clock pins.
reference FFRD sch 0.5

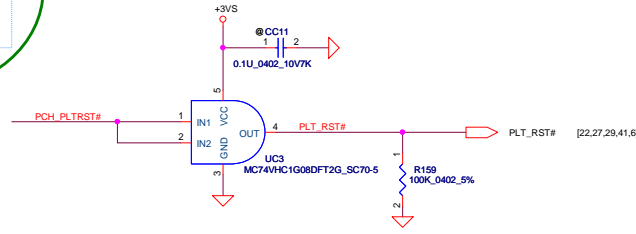


Latitude Oak Modified

PCH_PLTRST#
CC33 ESD@
0.047U_0402_16V4Z
Place CC33 close to UC3.1 & UC3.2



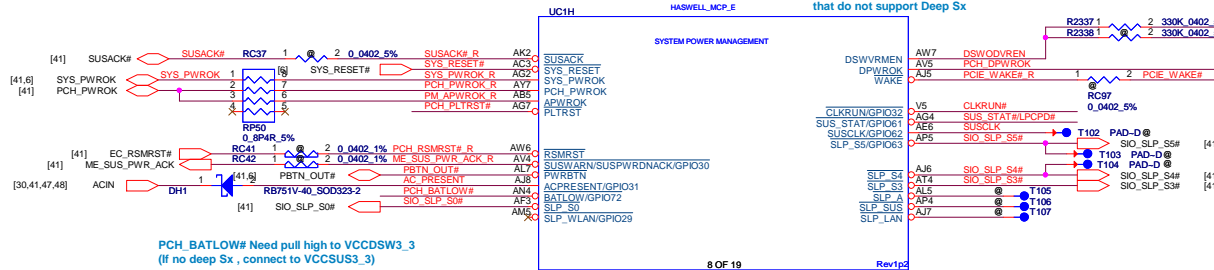
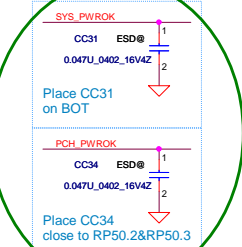
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC, if not support Deep Sx



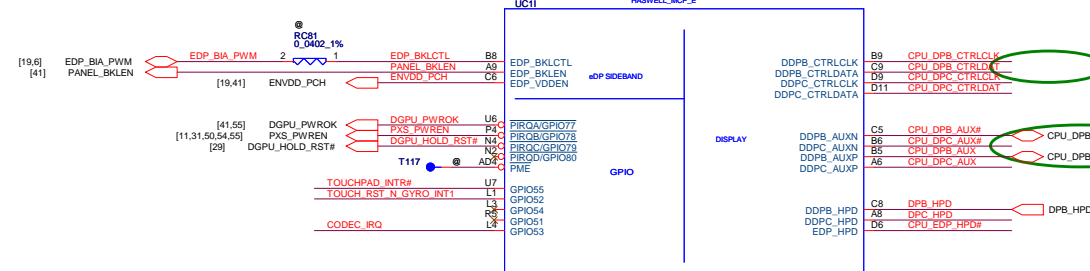
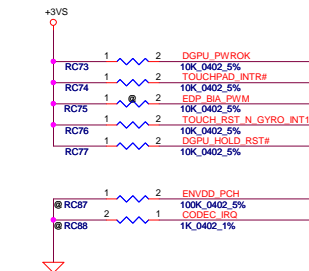
DSWODVREN - On Die DSW VR Enable
* H : Enable(DEFAULT)
L : Disable

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

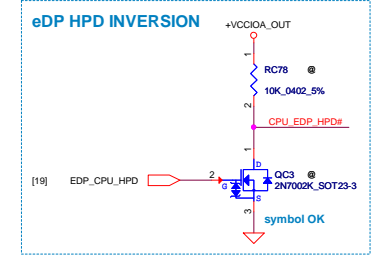
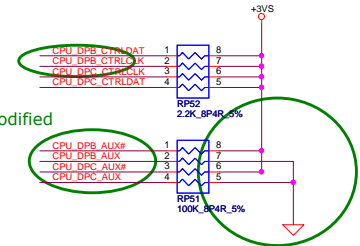
Latitude Oak Modified



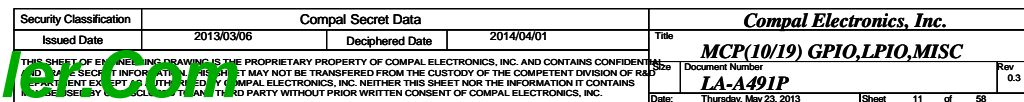
PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx, connect to VCCSUS3_3)

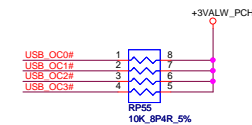


Latitude Oak Modified



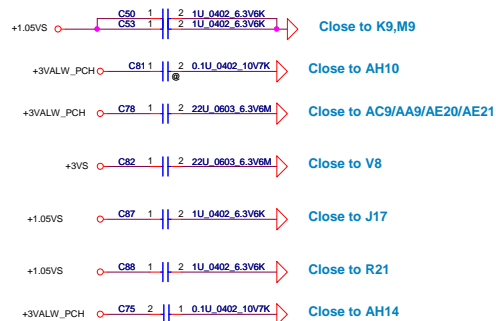
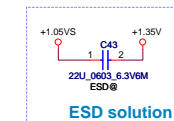
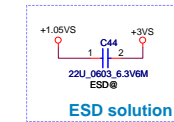
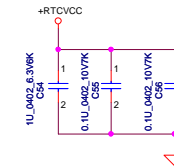
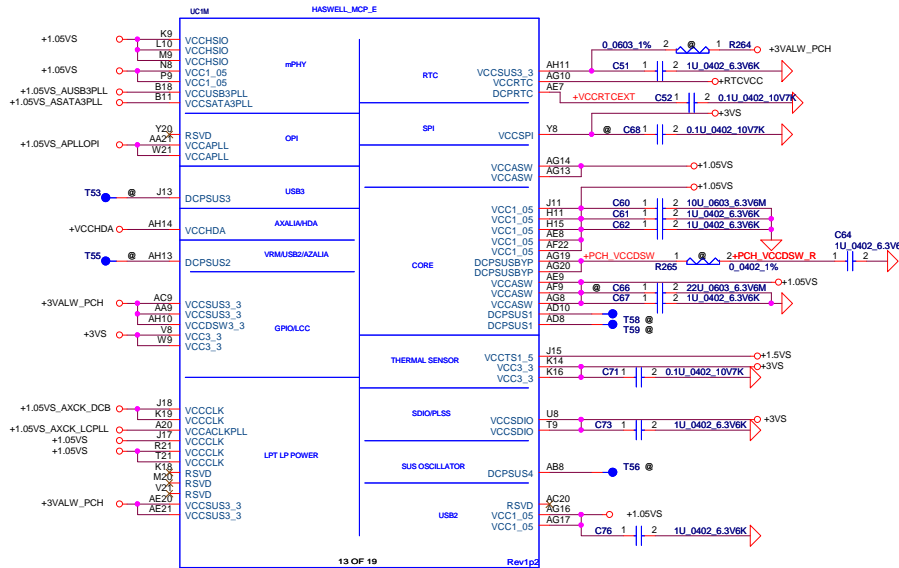
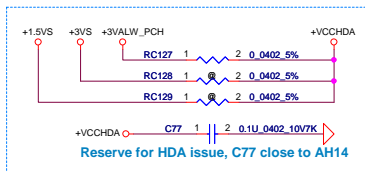
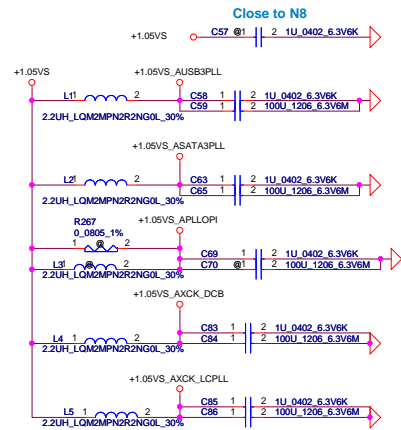
EDP_CPU_HPD 1 2 CPU_EDP_HPD# 0.0402_5% Reserve for eDP

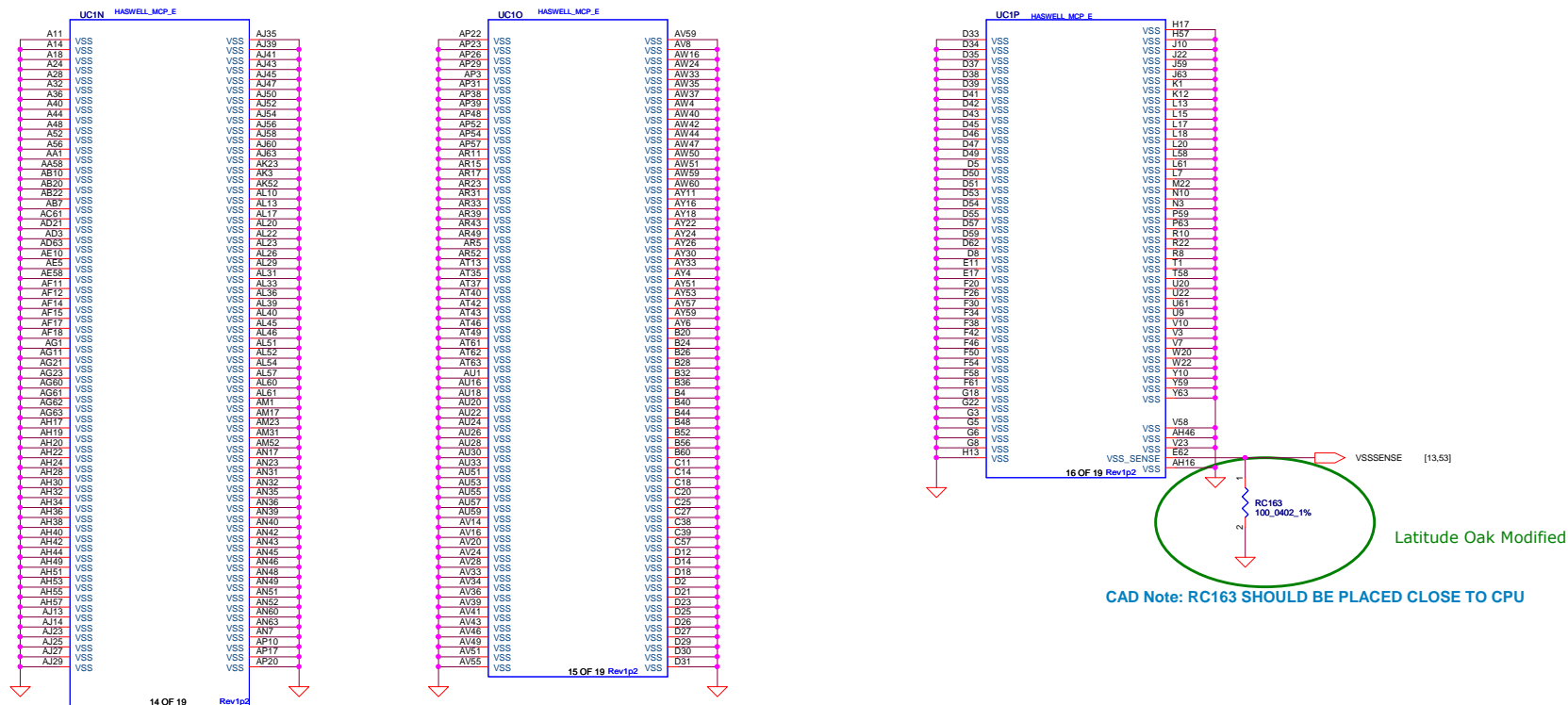




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Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

[7] DDR_A_DQS#0..7
[7] DDR_A_DQ0..63
[7] DDR_A_DQS#0..7
[7] DDR_A_MA0..15

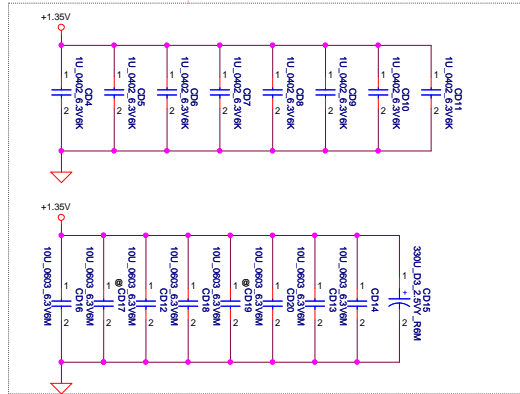
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

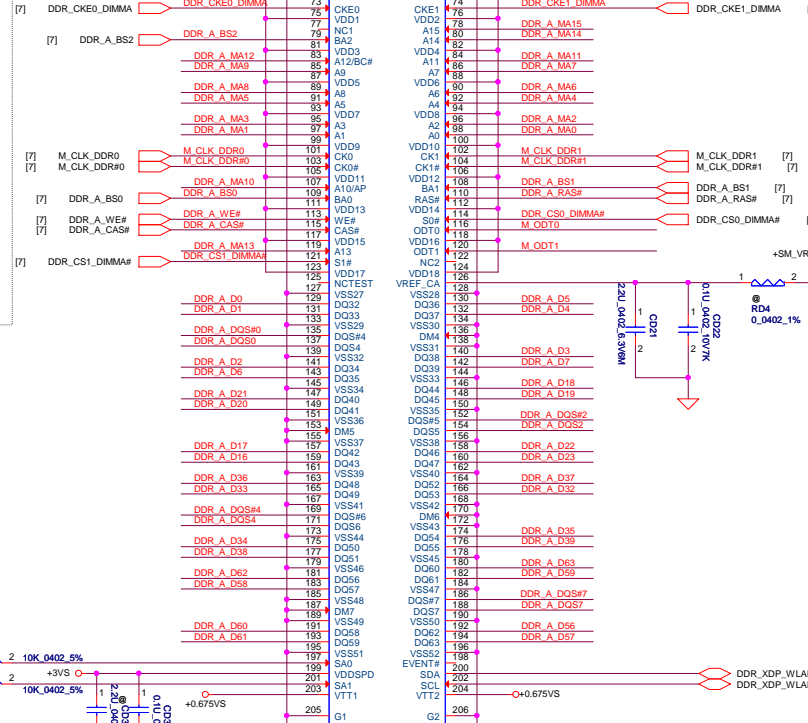
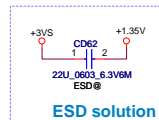
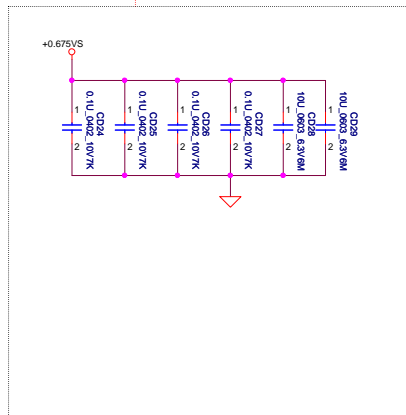
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

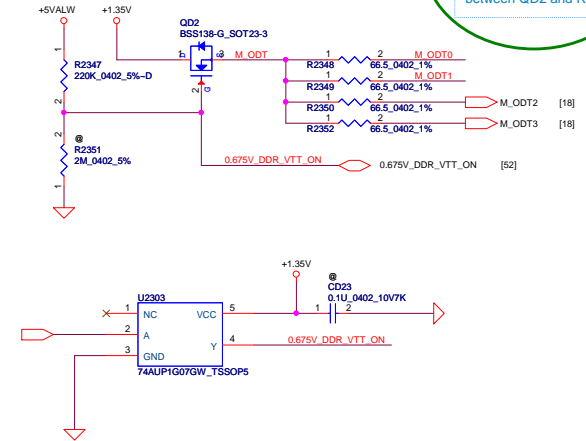
[18] DDR3_DRAMRST# [6] DDR3_DRAMRST#_CPU



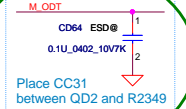
Layout Note:
Place near JDIMM1.203,204



DDR3L SODIMM ODT GENERATION



Latitude Oak Modified

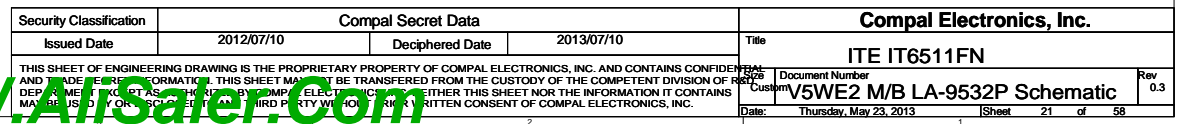


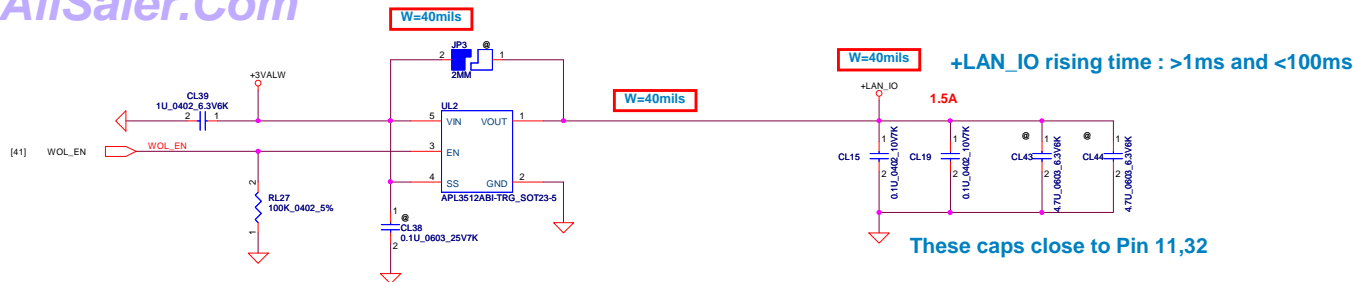
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2013/03/06		2014/04/01		eDP to LVDS converter	
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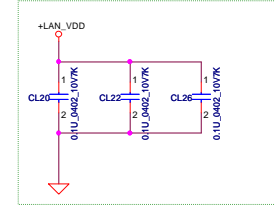
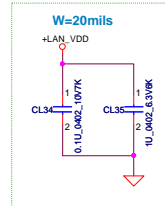


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Date	Thursday, May 23 2013	Sheet	20 of 58		

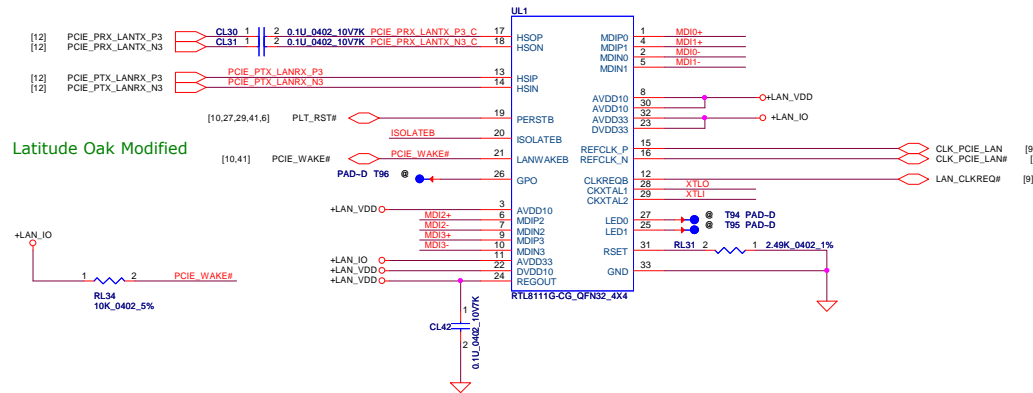




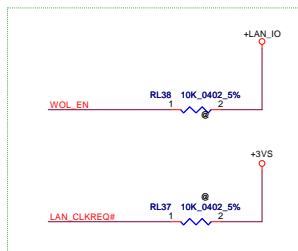
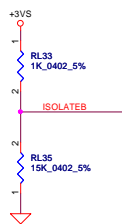
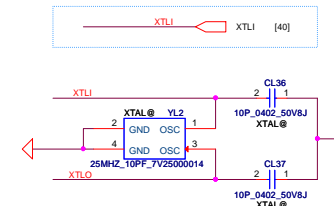
Latitude Oak Modified



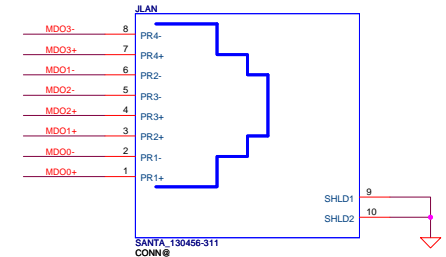
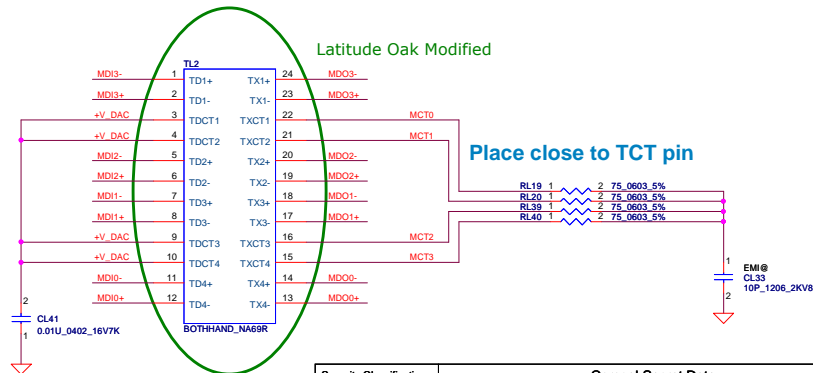
CL30, CL31 close to UL1 Pin 17, 18



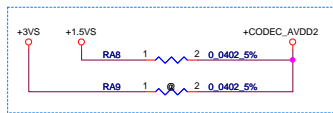
For GCLK



Reserve 10K pull

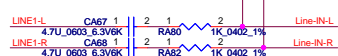
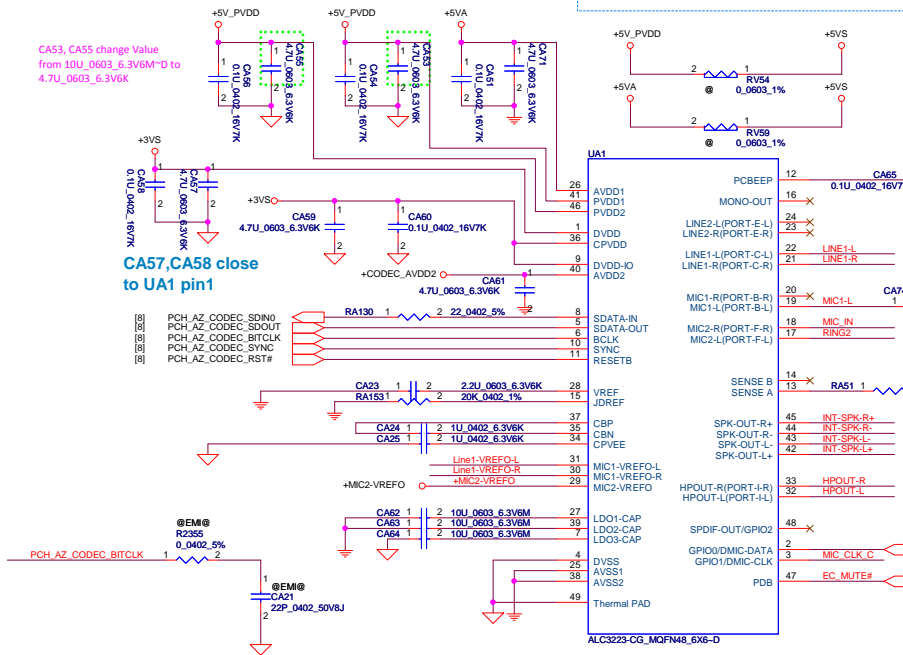


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Date: Thursday, May 23, 2013				Sheet	22 of 58

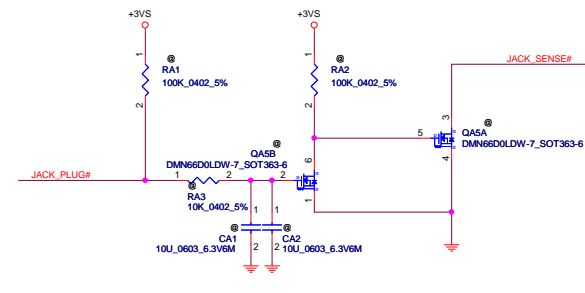


CA71, CA51 place close to Pin 26

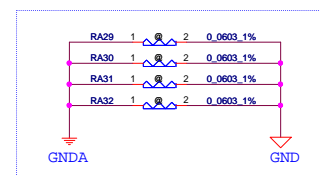
CA53, CA55 change Value from 10U_0603_6.3V6K to 4.7U_0603_6.3V6K



JACK_PLUG Delay circuitis

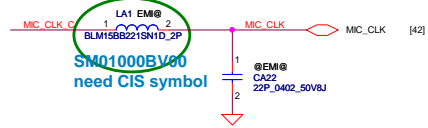


Reserve for cancel Delay circuitis

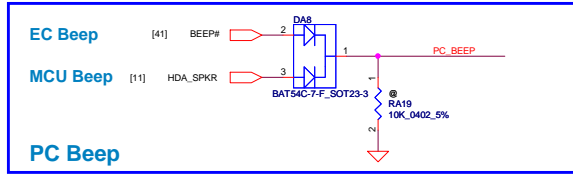


Place on the moat between GND & GNDA.

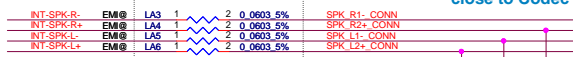
Latitude Oak Modified



SM01000BV00 need CIS symbol



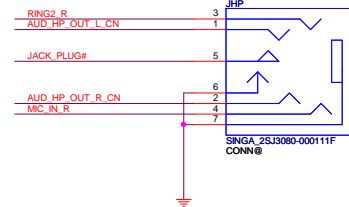
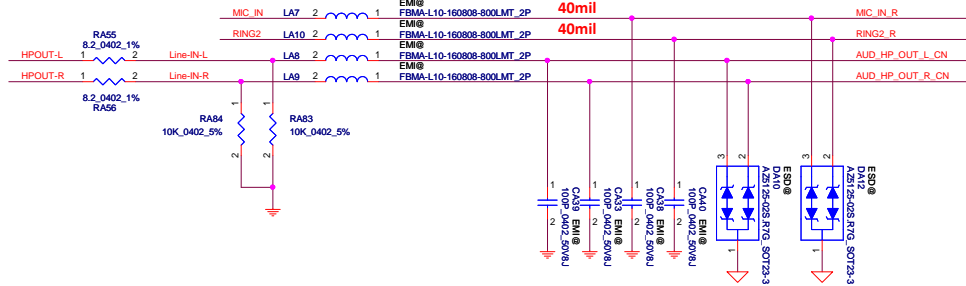
Close to UA1 Pin11,13,14,16



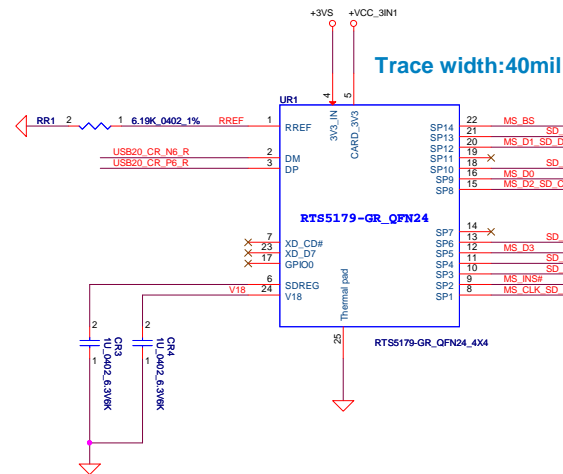
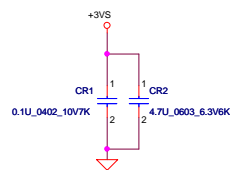
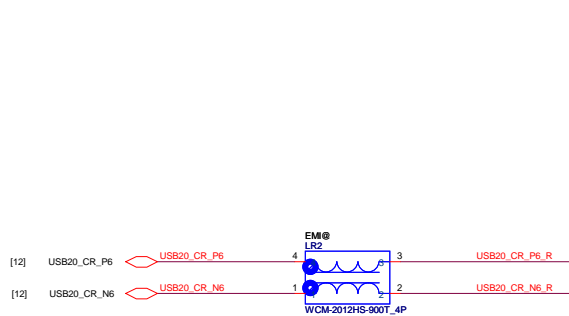
close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

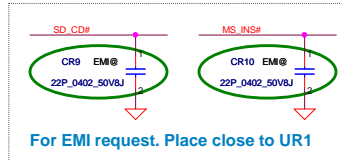
iPhone and Nokia type Combo Jack



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				Audio Codec ALC3223			
				Docuement Number			
				LA-A491P			
				Rev			
				0.3			
Date:				Thursday, May 23, 2013		Sheet 23 of 58	

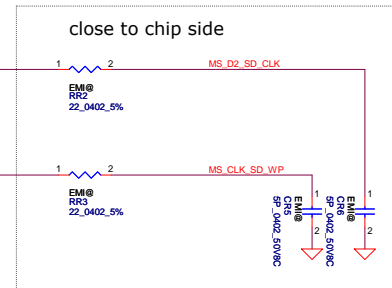
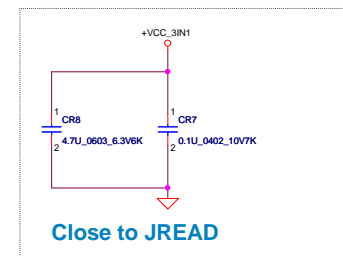


Latitude Oak Modified



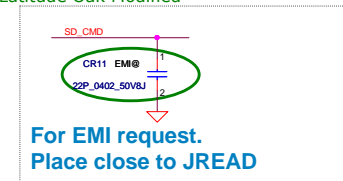
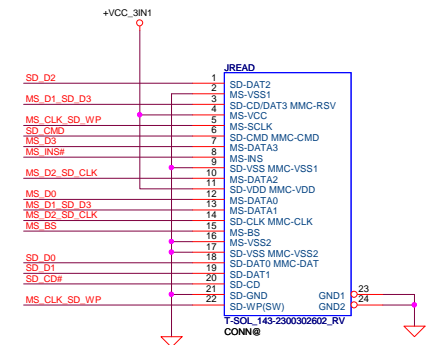
For EMI request. Place close to UR1

close to chip side

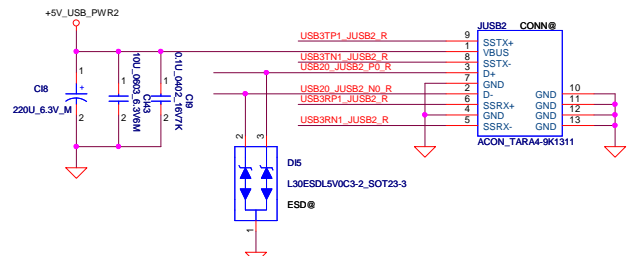
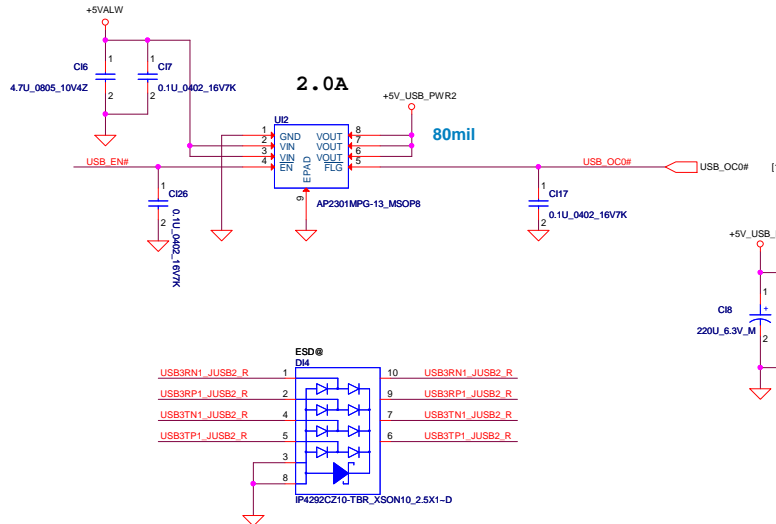
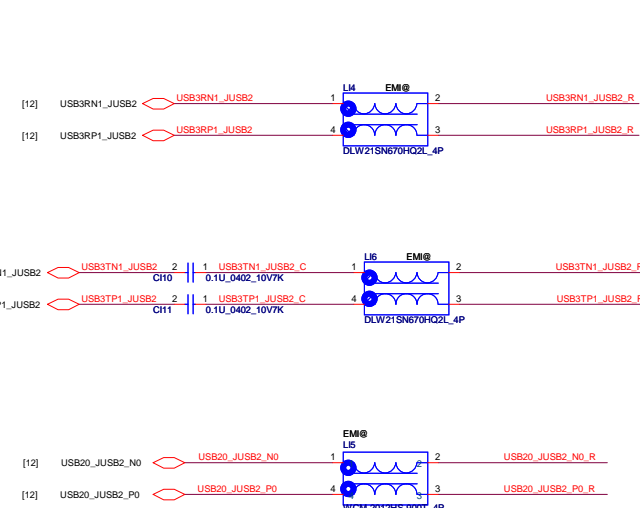
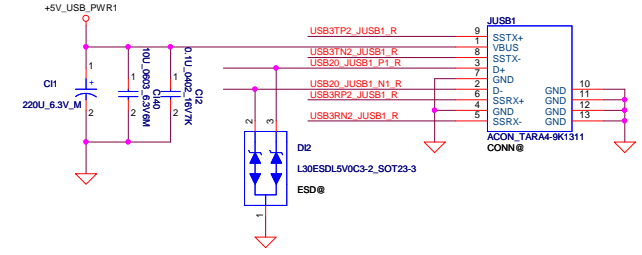
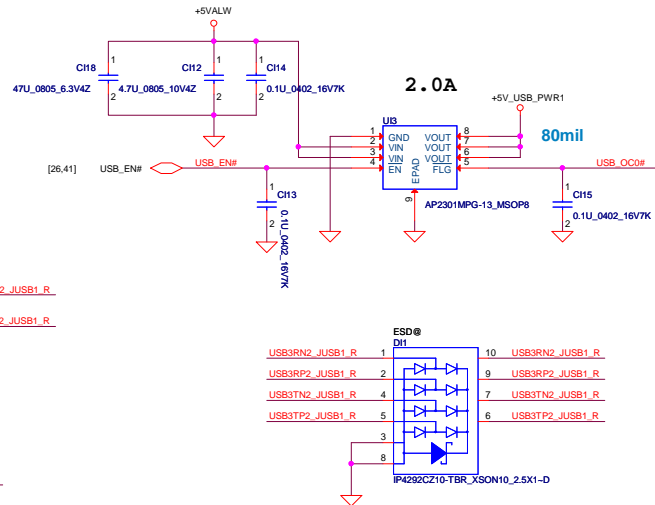
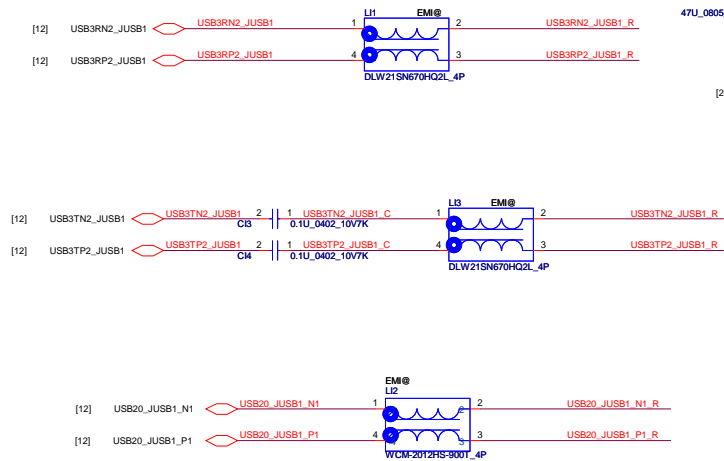
拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

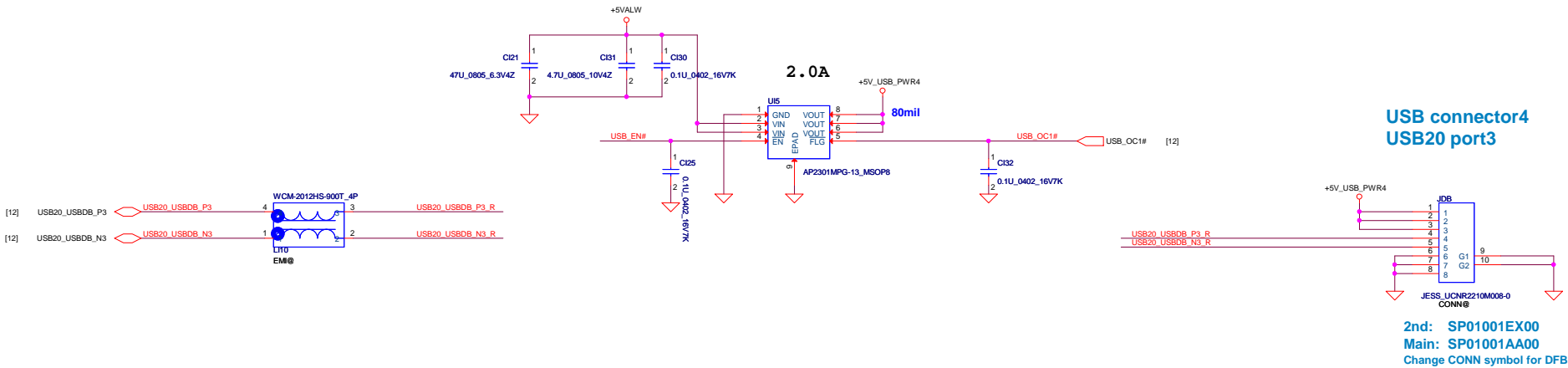
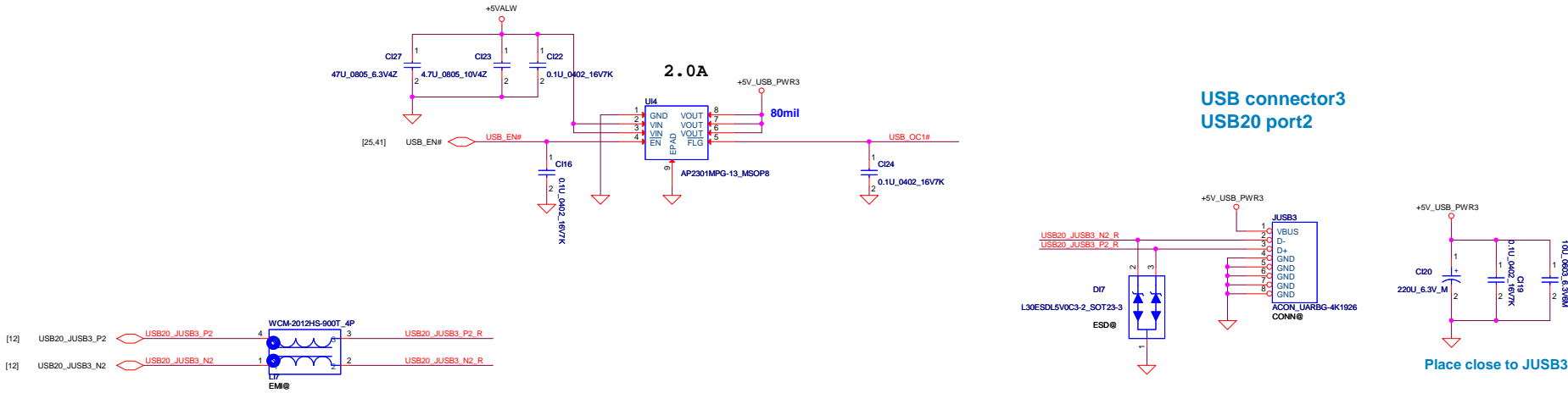
Close to JREAD

Latitude Oak Modified

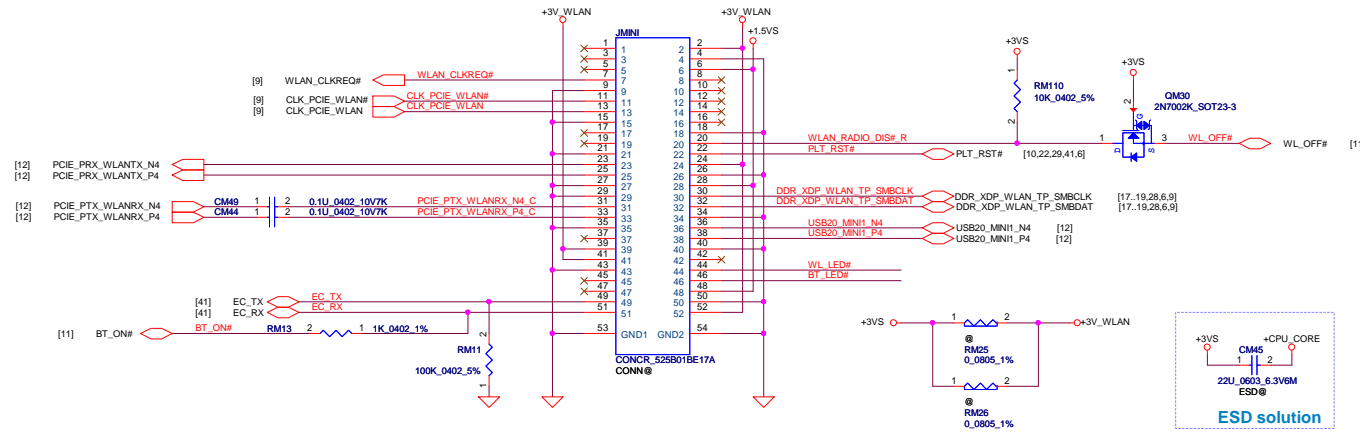
For EMI request.
Place close to JREAD

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Document Number	
2013/03/06		2014/04/01		LA-A491P	
Date		Thursday, May 23, 2013		Sheet 24 of 58	
Rev		0.3		Card Reader RTS5179	
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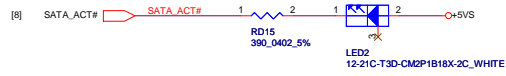




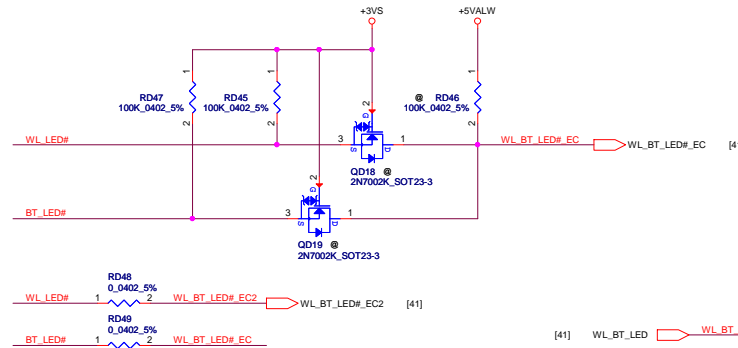
Mini WLAN/WIMAX H=6.7



HDD LED



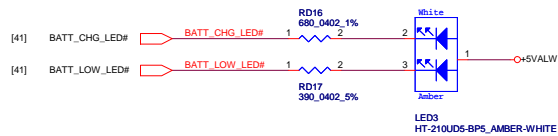
10mils, All pins



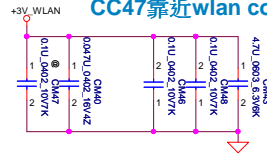
Power LED



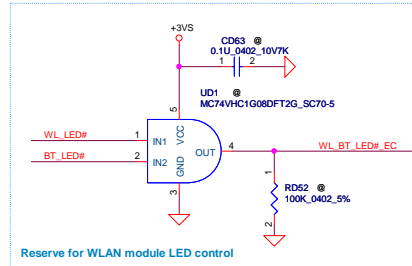
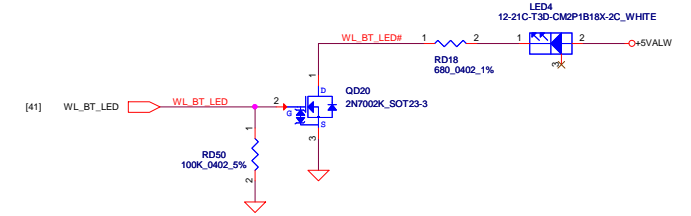
Battery LED



CC47靠近wlan connector

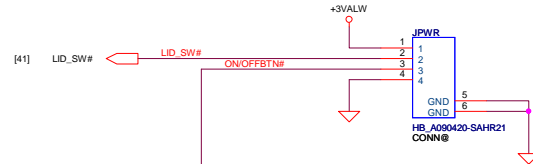


Wireless LED



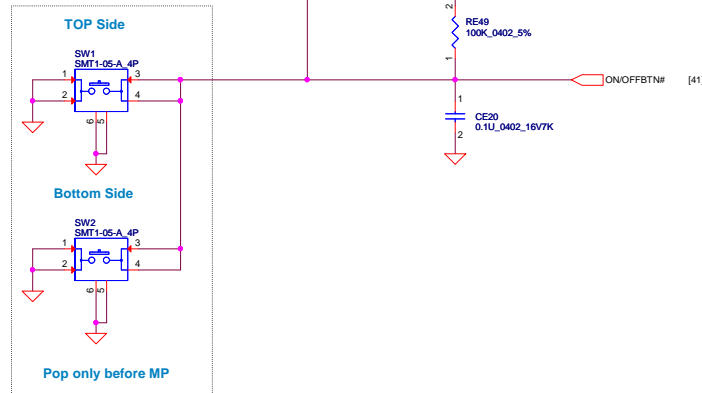
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	Mini Card/LED
Document Number				Rev	0.3
Date				Thursday, May 23, 2013	Sheet 27 of 58

POWER/B

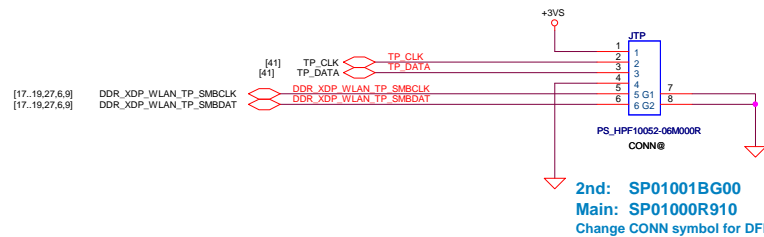


Power ON Circuit

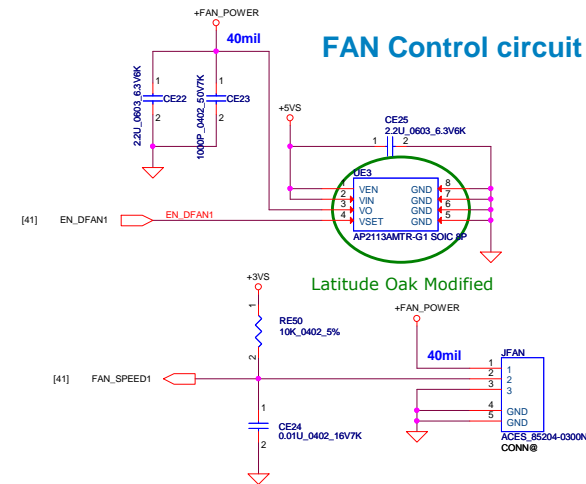
ON/OFF switch



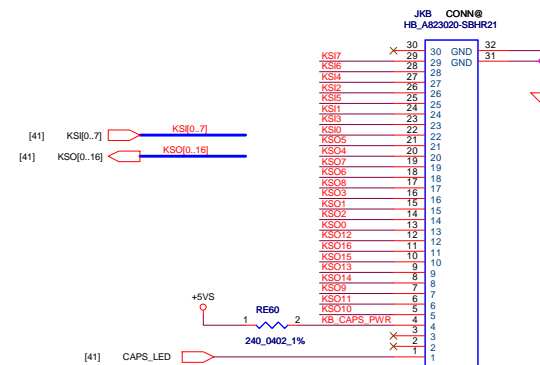
Touch pad



FAN Control circuit

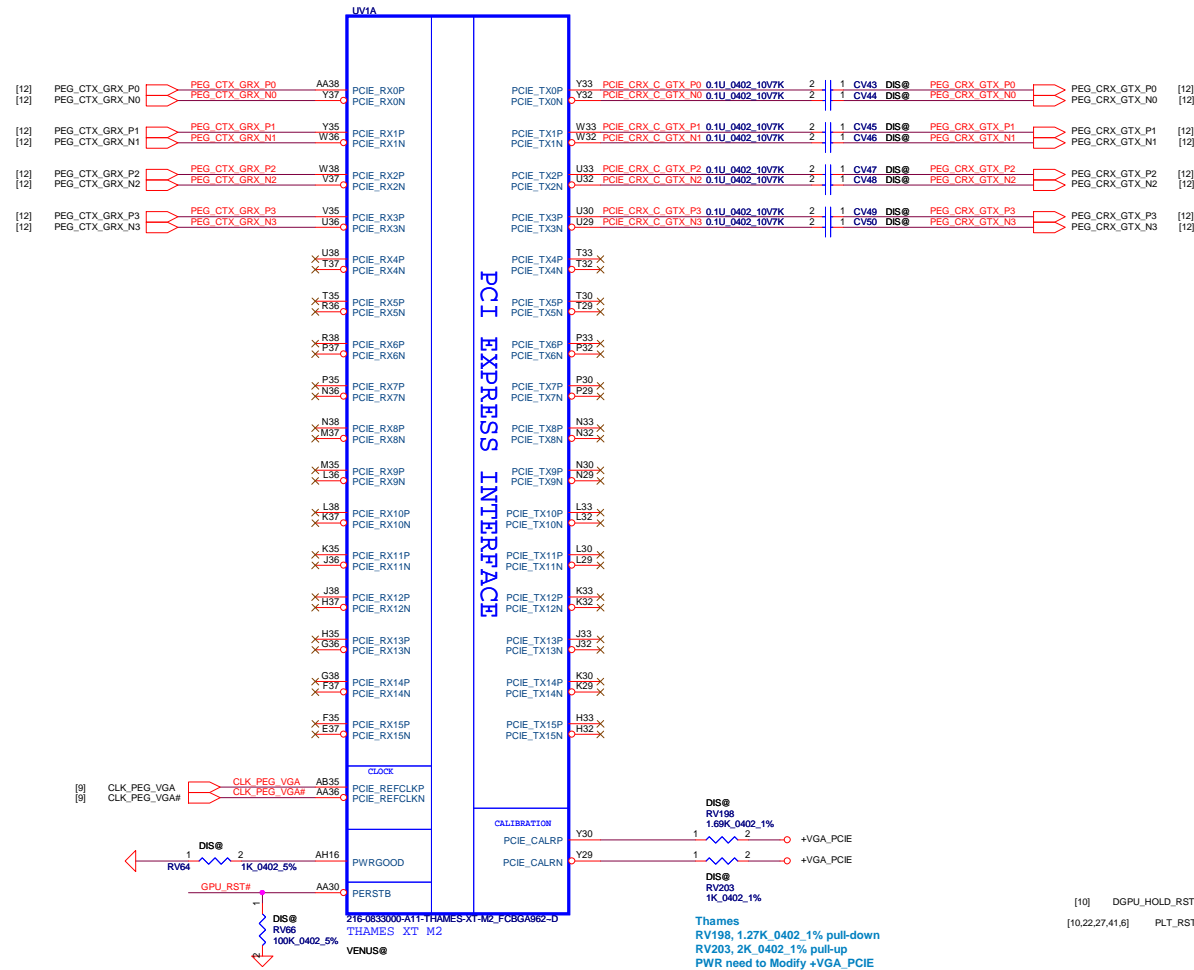


INT_KBD Connector

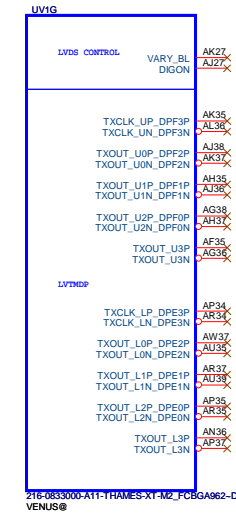


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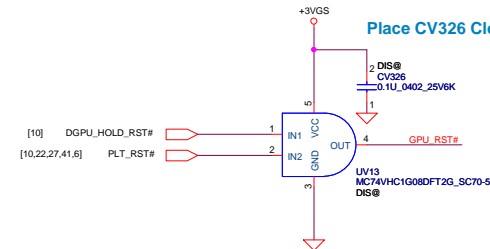
GFX PCIE LANE REVERSAL



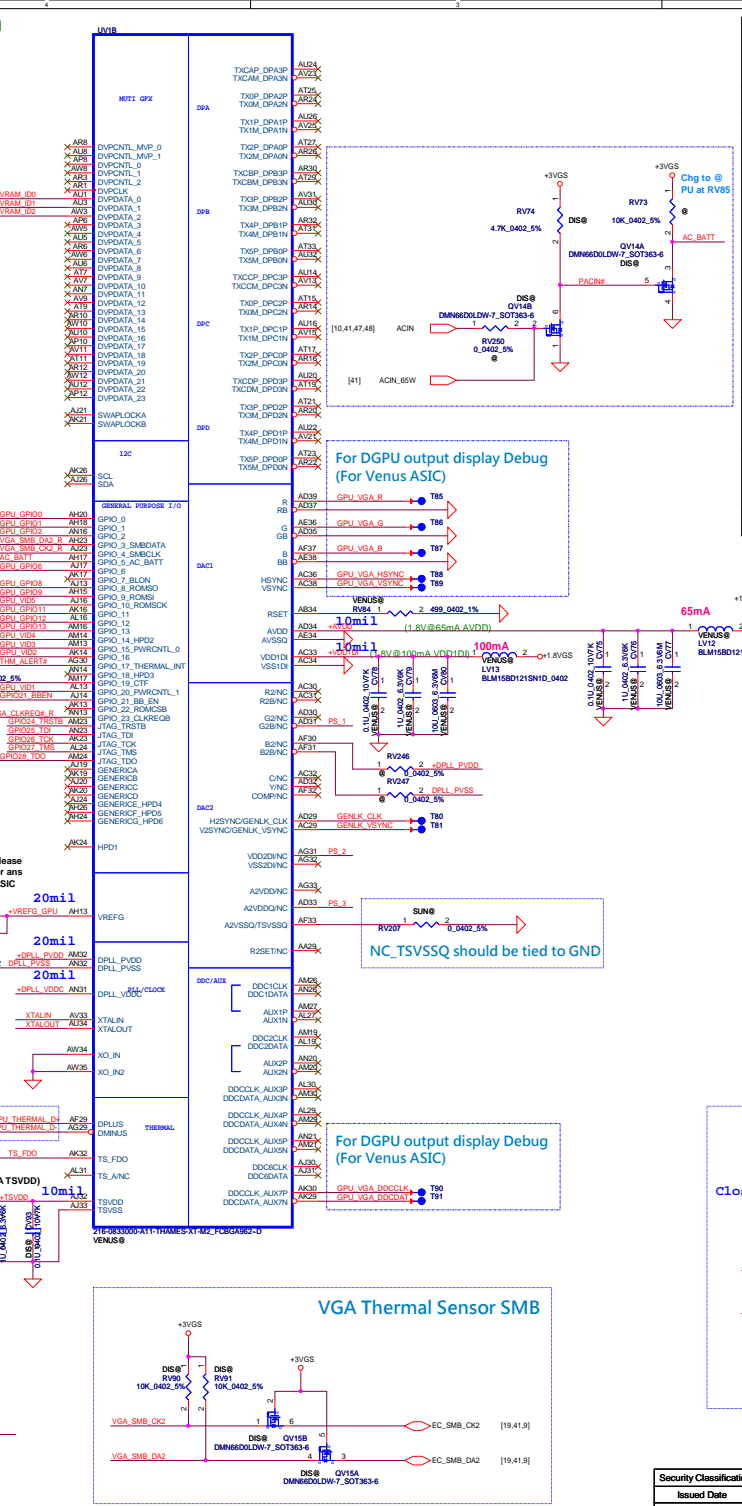
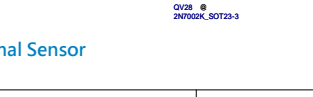
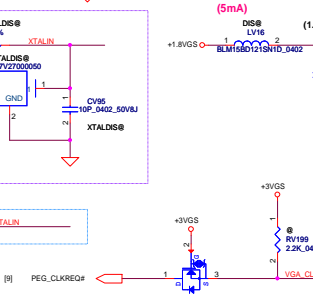
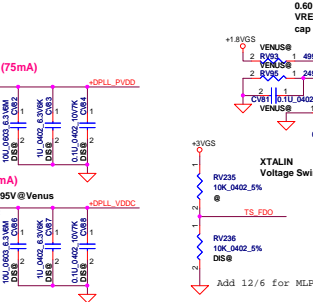
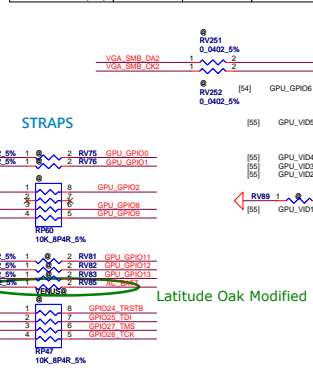
LVDS Interface



Place CV326 Close to UV13



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID
AS0002044R-12C Hynix 2Gb SA00004GD1L(R1) SA00004GD2L(R3) AS0001044R-12C Samsung 2Gb SA00005B70L(R1) SA00005B71L(R3)	RV67 1	RV69 1	RV71 1
AS0001044R-12C Samsung 2Gb SA00005B70L(R1) SA00005B71L(R3)	RV68 6	RV69 1	RV71 1
	RV67 1	RV70 0	RV71 1
AS0002039R-11C Hynix 2Gb SA000006H40L(R1) SA000006H41L(R3) AS0001044R-12C Samsung 2Gb SA00005SH0L(R1) SA00005SH1L(R3) AS0001044R-12C Micron 2Gb SA00005X80L(R1) SA00005X81L(R3)			



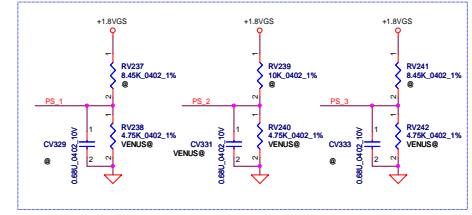
CONFIGURATION STRAPS				RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEFENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIe FULL TX OUTPUT SWING	0: 50% swing 1: Pull enable	X
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Adjustment POLE speed when compliance test	0: 5,502/s 1: 502/s	0
RSVD	GPIO8	RESERVED		0
BUF_VGA_DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_32_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		xxx
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	HS2SYNC			0
RSVD	GENERICC			0
AUD[1]	HSYNC	AUD[1] (AUDIO) 0/0 No audio function 0/1 Audio for DisplayPort and HDMI if dongle is detected 1/0 Audio for DisplayPort only 1/1 Audio for both DisplayPort and HDMI		11
AUD[0]	V2SYNC			

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

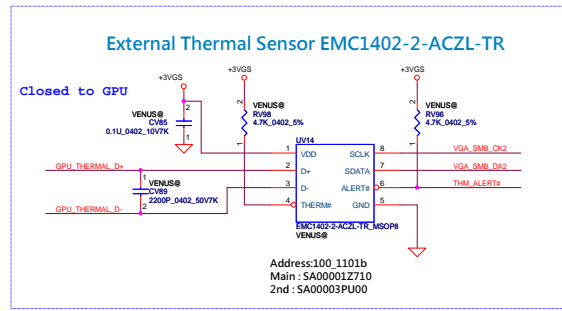
GPIO21	HS2SYNC	GENERICC	GPIO2	GPIO8
--------	---------	----------	-------	-------

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



ION MLPs PS_3	RV241	RV242	Bits [3:-1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

VENUS MLPs
PS_3 used default

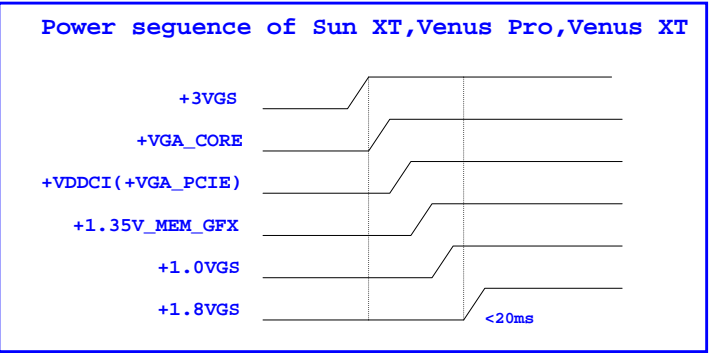
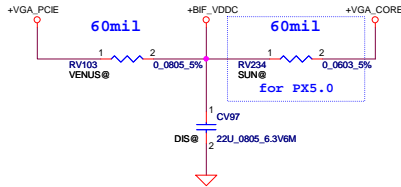
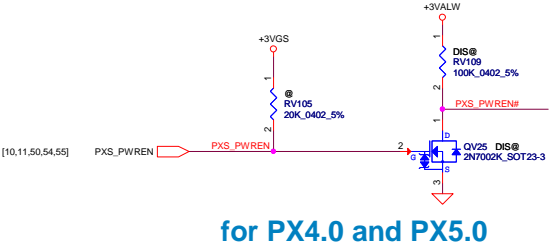


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Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	ATI Vender Pro M2 Main MSIC
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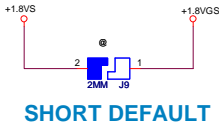
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3,PCIE_VDDC and 1.8V rail

Note:
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

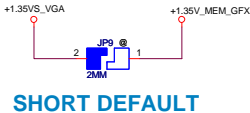
Switch circuits in BACO desings for Thames/Seymour only
55mA@1.0V, in BACO mode



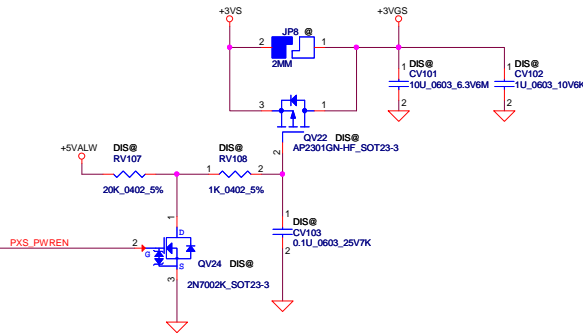
+1.8VS TO +1.8VGS

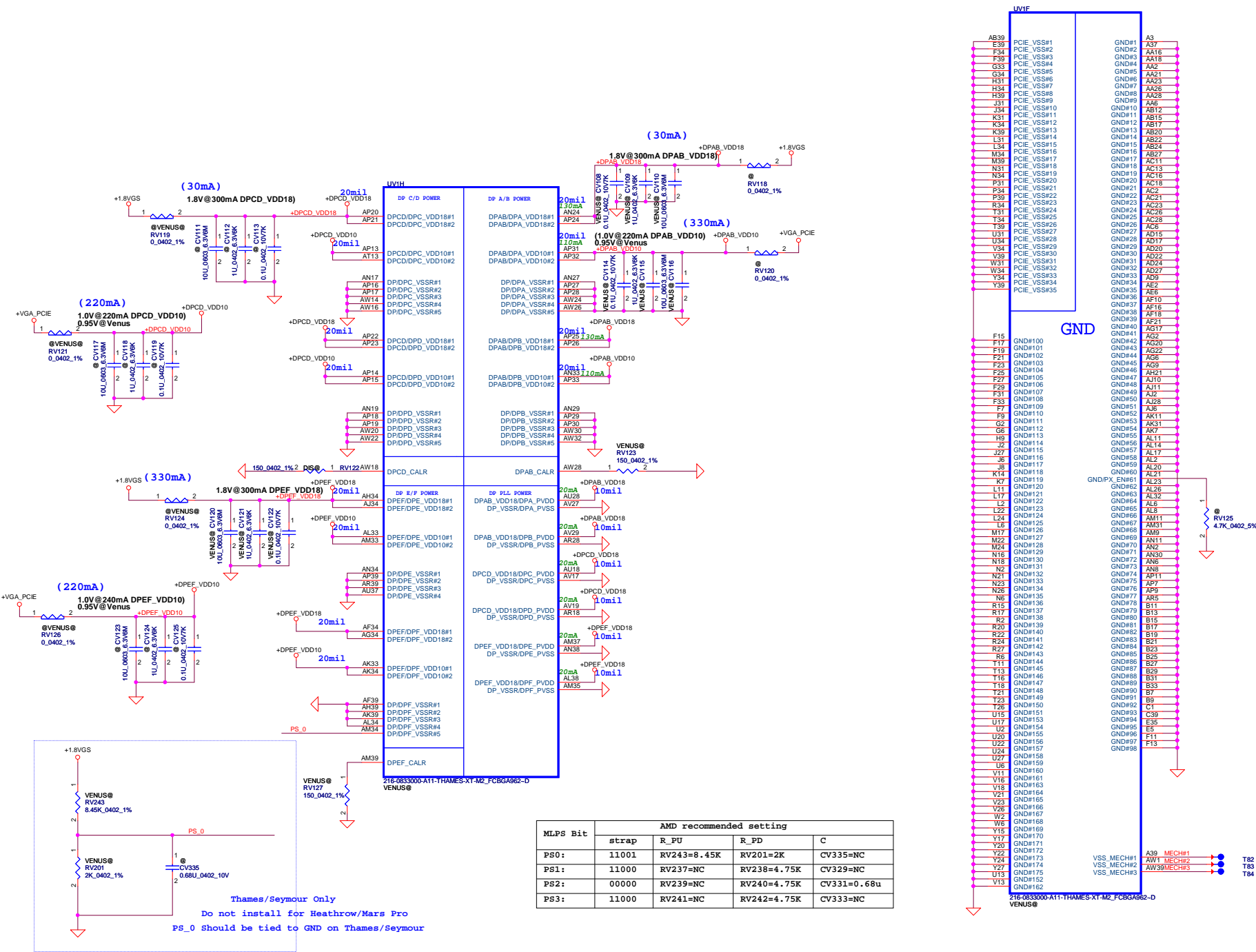


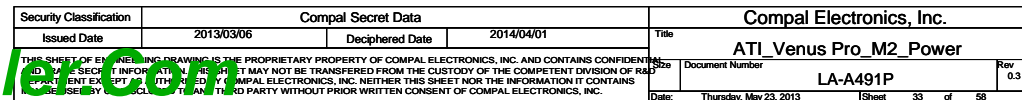
+1.35VS_VGA TO +1.35V_MEM_GFX

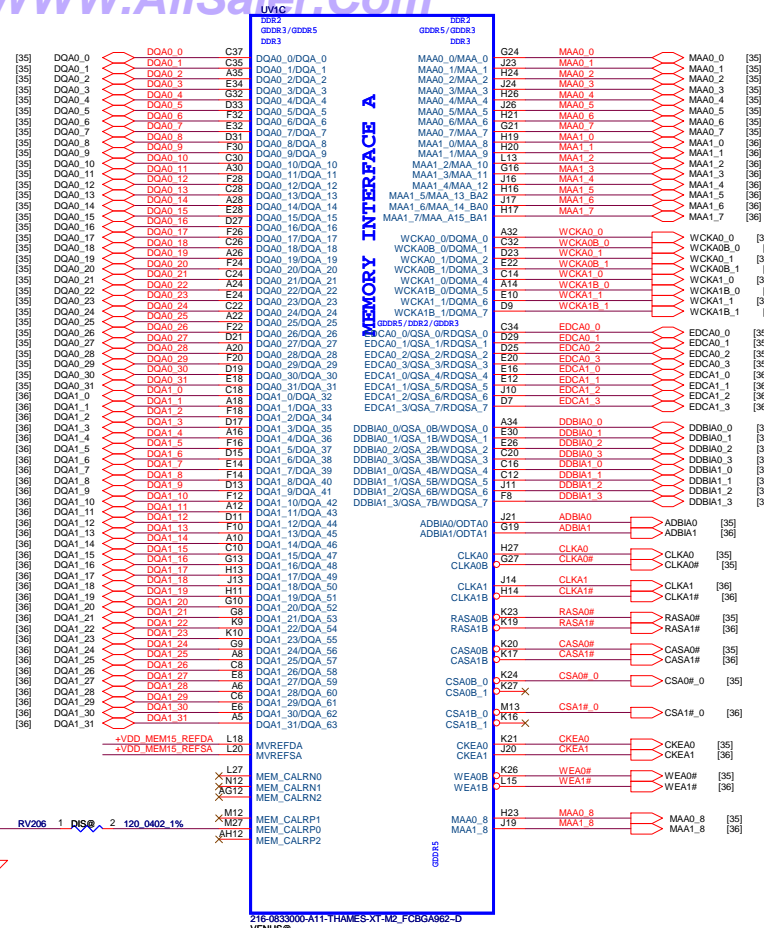


+3VS TO +3VGS



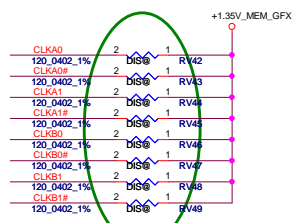




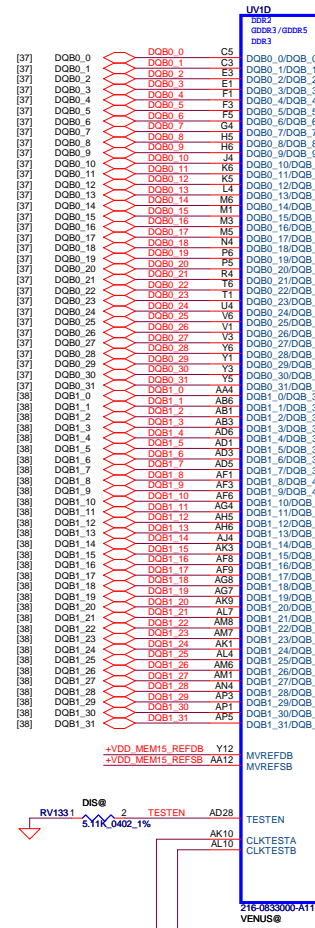


GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD6	CS#
CMD8	CMD18	ABIS#
CMD10	CMD20	A0_A10
CMD11	CMD21	A1_A9
CMD12	CMD22	A2_BA0
CMD13	CMD23	A3_BA3
CMD14	CMD24	A4_BA4
CMD15	CMD25	A5_BA1
CMD16	CMD26	A6_A11
CMD17	CMD27	A7_A11
CMD18	CMD28	A12_FRU
CMD19	CMD29	CKE#
CMD20	CMD30	RESET#
CMD21	CMD31	

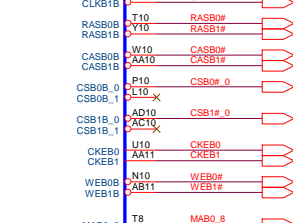


Latitude Oak Modified

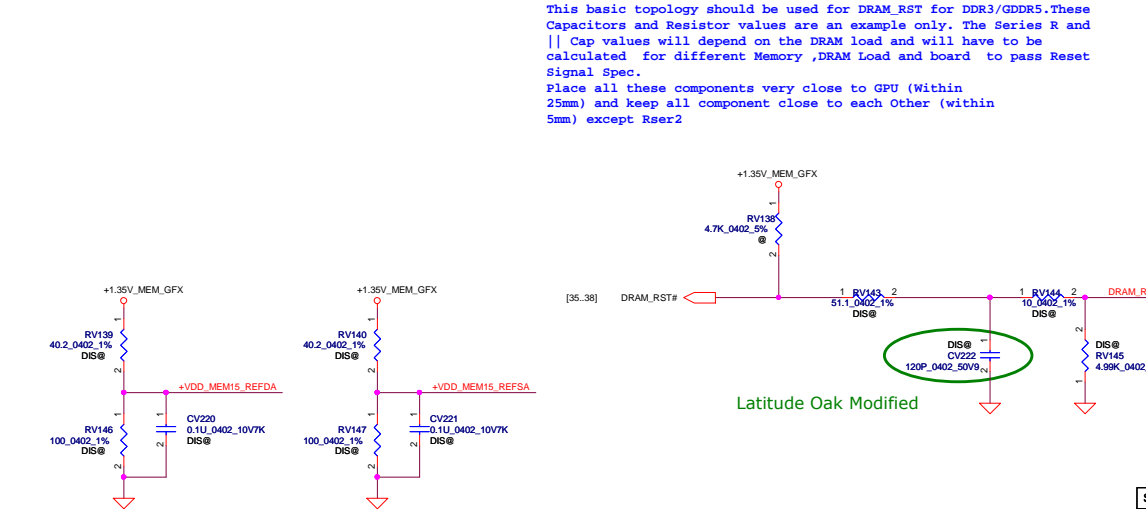


GDDR5 CMD Mapping Table

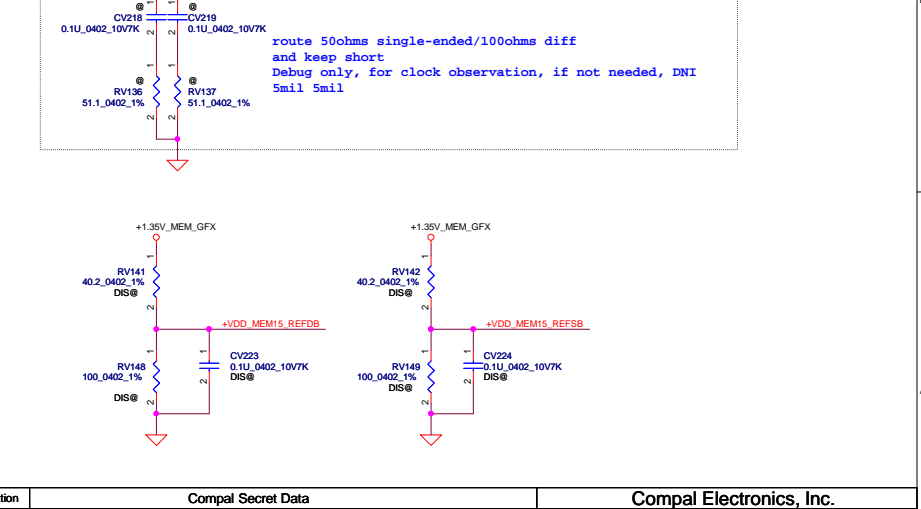
<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD6	CS#
CMD8	CMD18	ABIS#
CMD10	CMD20	A0_A10
CMD11	CMD21	A1_A9
CMD12	CMD22	A2_BA0
CMD13	CMD23	A3_BA3
CMD14	CMD24	A4_BA4
CMD15	CMD25	A5_BA1
CMD16	CMD26	A6_A11
CMD17	CMD27	A7_A11
CMD18	CMD28	A12_FRU
CMD19	CMD29	CKE#
CMD20	CMD30	RESET#
CMD21	CMD31	

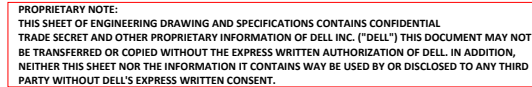


Latitude Oak Modified



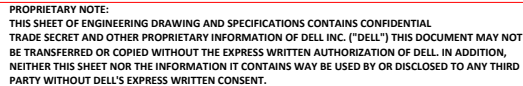
Latitude Oak Modified





Compal Electronics, Inc.

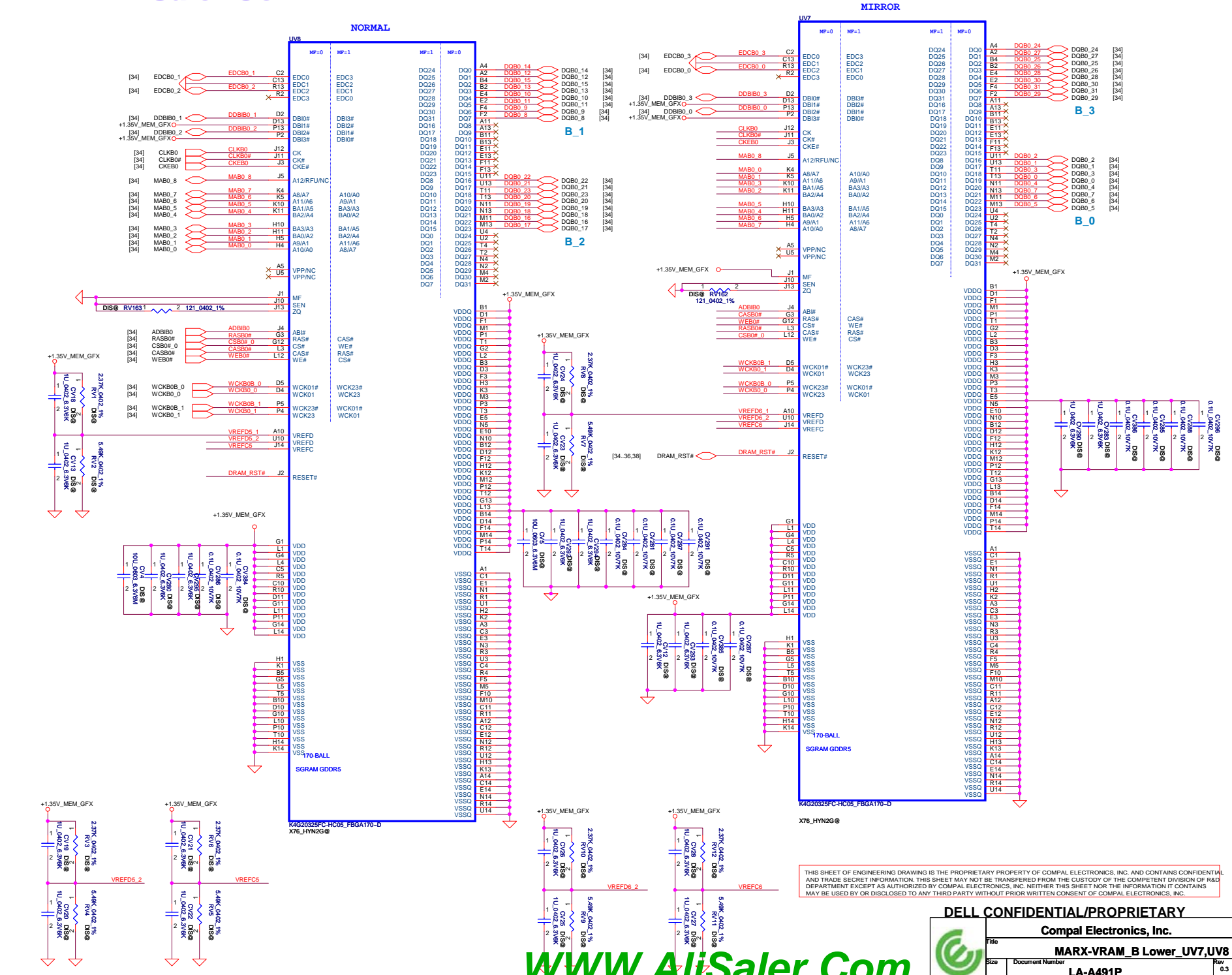
Title			
VRAM_A Lower_UV4,UV5			
Size	Document Number	Rev	
	LA-A491P	0.3	
Date:	Thursday, May 23, 2013	Sheet	35 of 58



Compal Electronics, Inc.

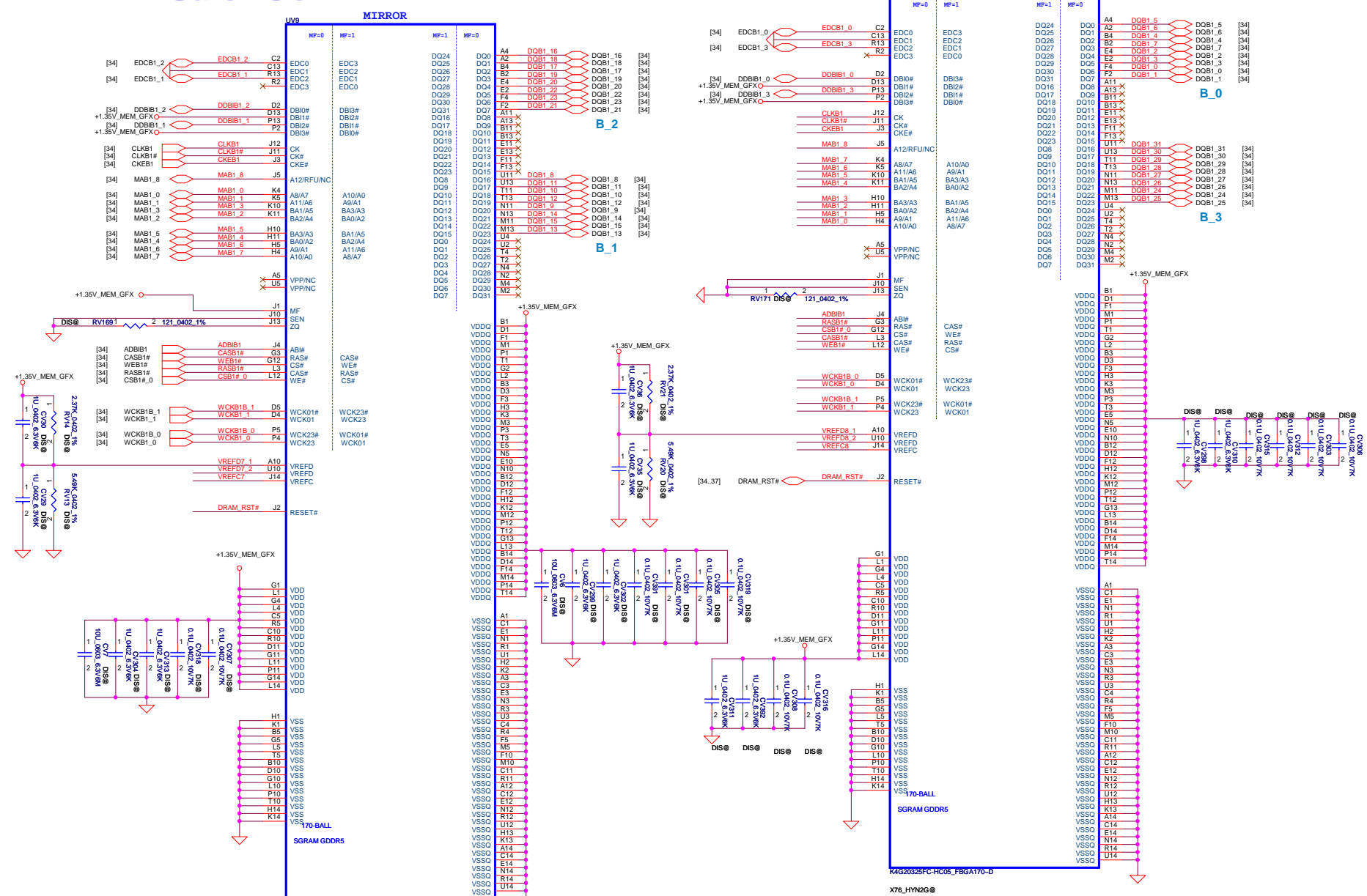
MARX-VRAM_A Upper_UV3,UV6		
Size	Document Number	Re

LA-A491P



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DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title		MARX-VRAM_B Lower_UV7,UV8	
Size	Document Number	LA-A491P	
Date	Thursday, May 23, 2013	Sheet	37 of 58

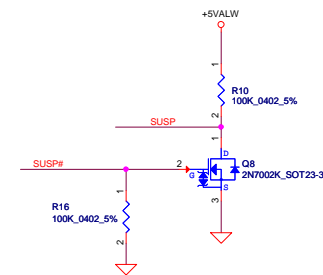
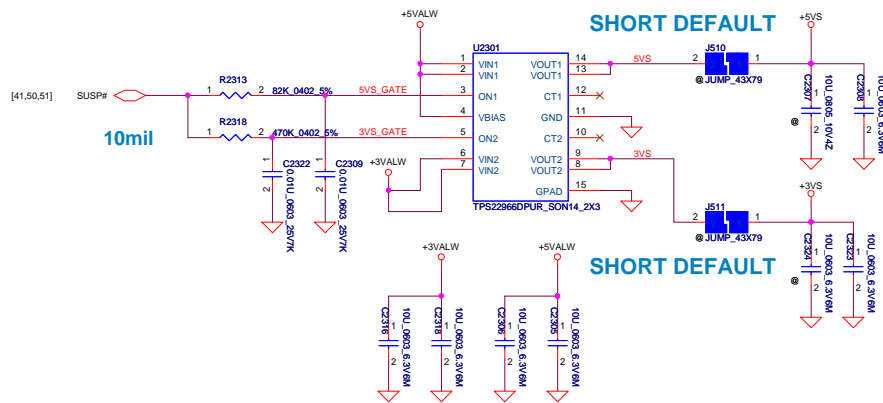


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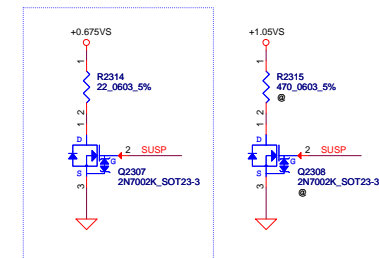
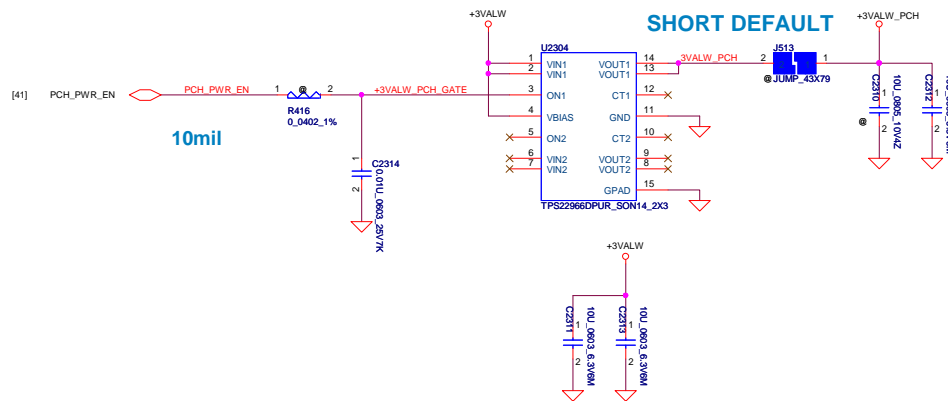
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
MARX-VRAM_B Upper_UV9,UV10	
Size	Document Number
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+5VS and +3VS switch

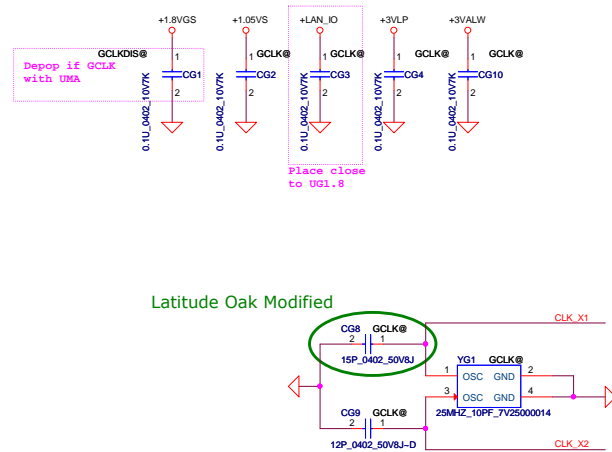


+3VALW_PCH switch



For Intel S3 Power Reduction

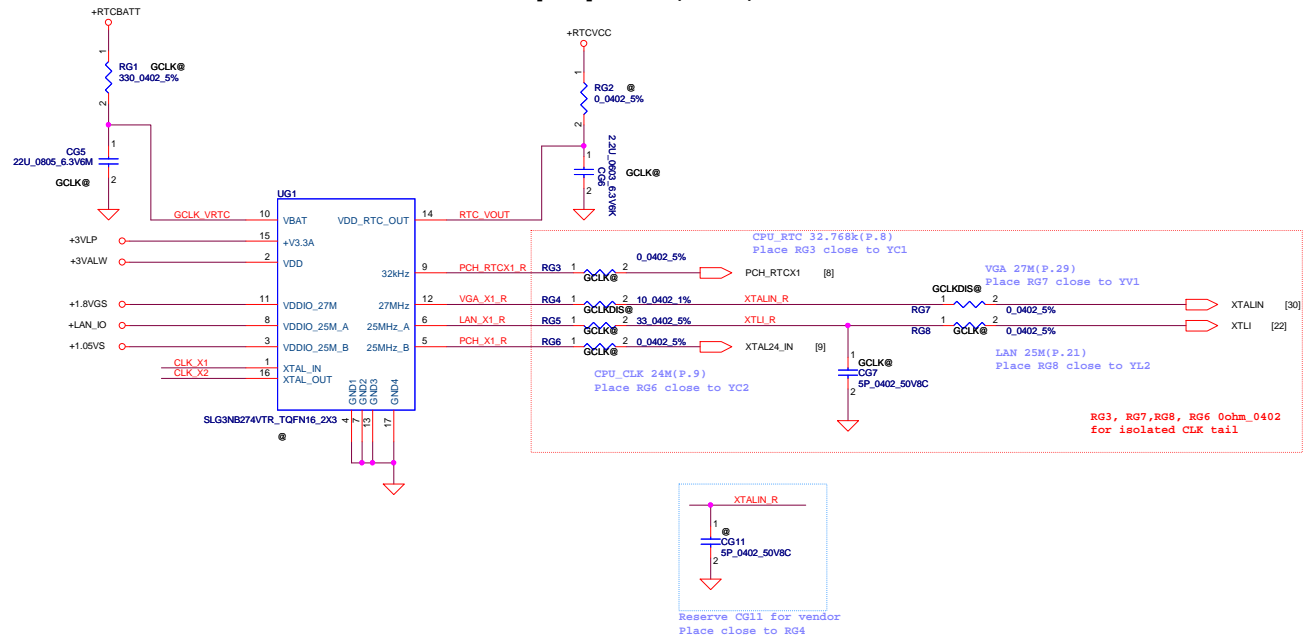
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	DC/DC Interface
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				Date	Thursday, May 23, 2013
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				Rev	0.3



UG1 GCLKUMA@
SLG3NB244VTR TQFN 16P CLK GEN

UG2 GCLKDIS@
SLG3NB244VTR TQFN 16P CLK GEN

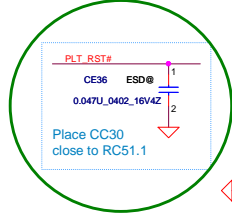
SLG3NB3374V is for DIS by output 24M*1, 25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M81, 25M*1, 32K*1



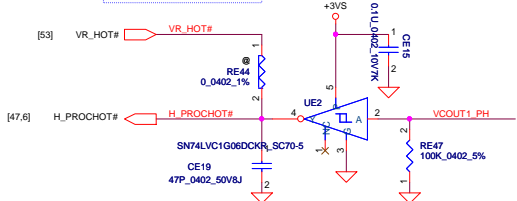
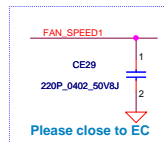
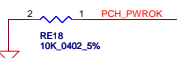
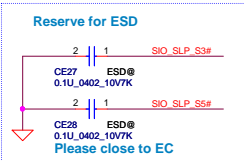
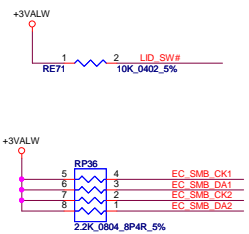
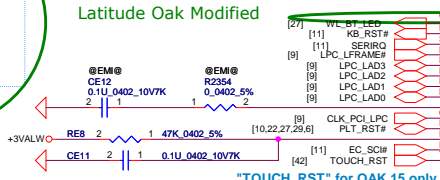
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	GCLK
Document Number				Rev	0.3
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SD034120280 12K_0402_1%
SD034270280 27K_0402_1%
SD034430280 43K_0402_1%
SD034560280 56K_0402_1%
SD034750280 75K_0402_1%
SD034100380 100K_0402_1%
SD034130380 130K_0402_1%
SD034200380 200K_0402_1%
SD00000G280 270K_0402_1%

Latitude Oak Modified

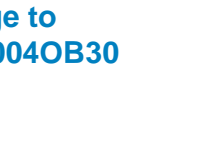
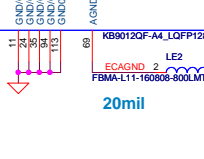
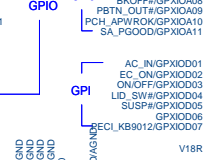
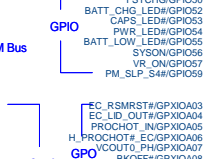
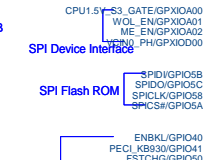
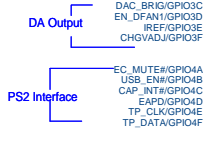
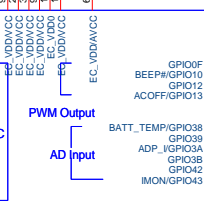
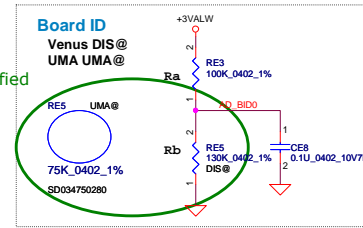


Latitude Oak Modified

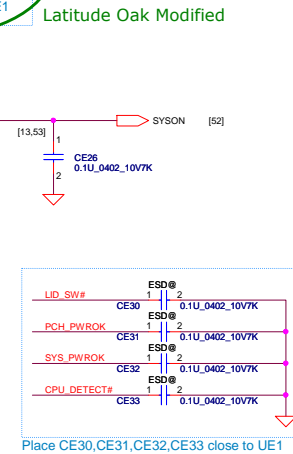
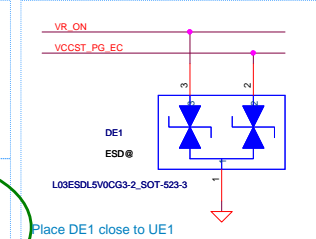
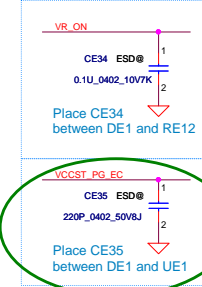
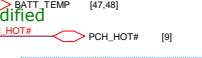


KB9012A3 change to
KB9012A4 SA000040B30

Latitude Oak Modified

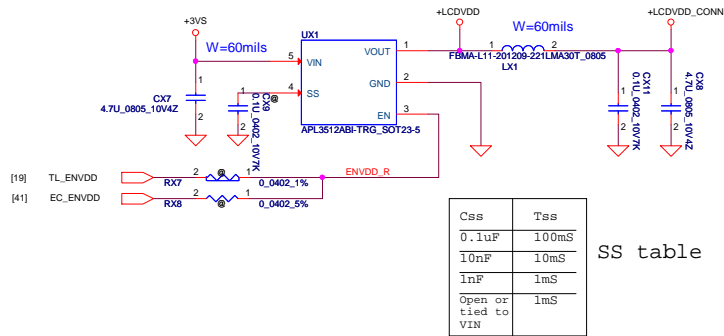


ME_FWP PCH has internal 20K PD.
(suspend power rail)

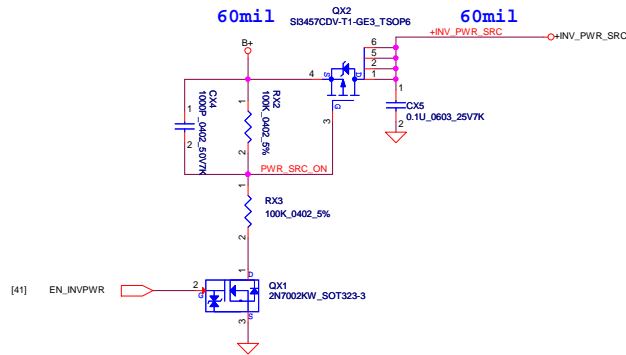


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2013/03/06		2014/04/01		Document Number	
				LA-A491P	
				Date	
				Thursday, May 23, 2013	
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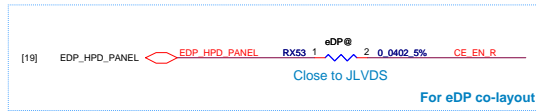
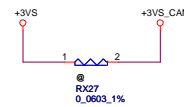
LCD PWR CTRL



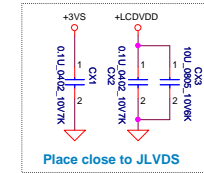
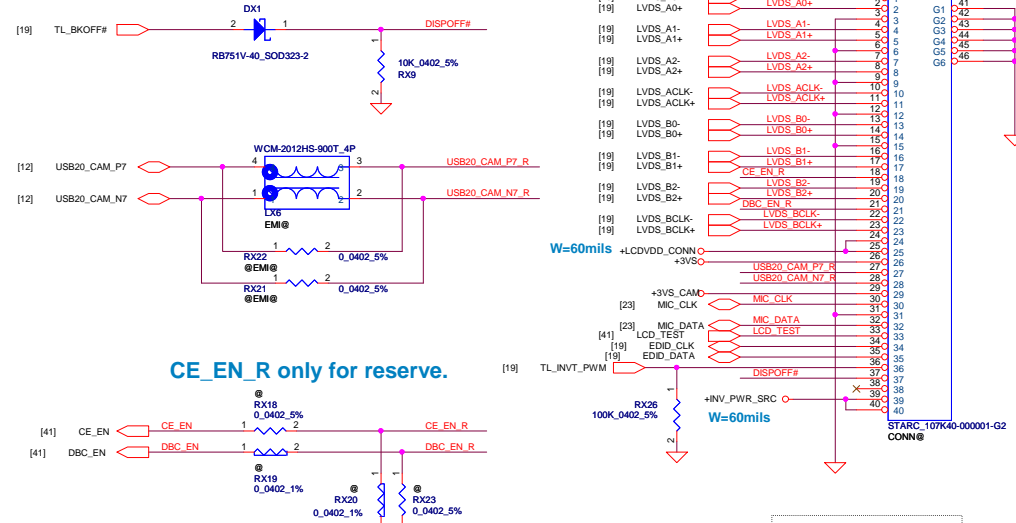
LCD backlight PWR CTRL



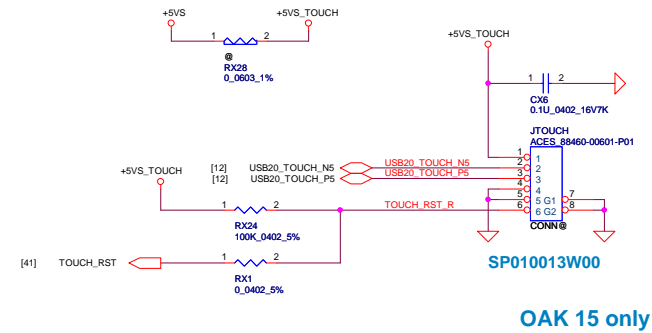
Webcam PWR CTRL



LVDS Connector

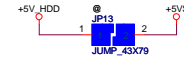


* Touch Screen Panel

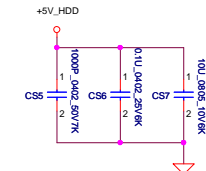
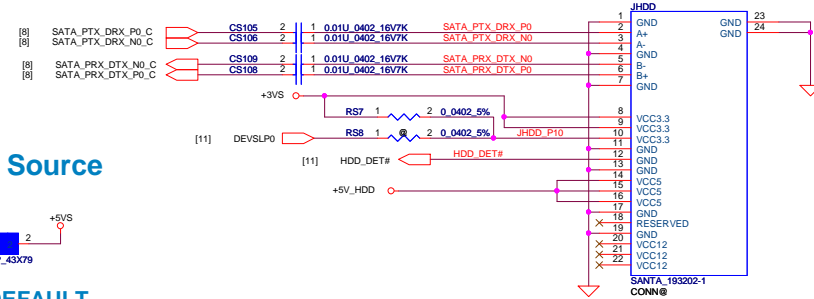


SATA HDD Connector

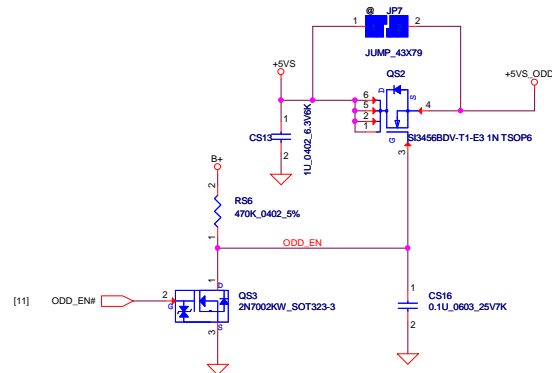
+5V_HDD Source



SHORT DEFAULT

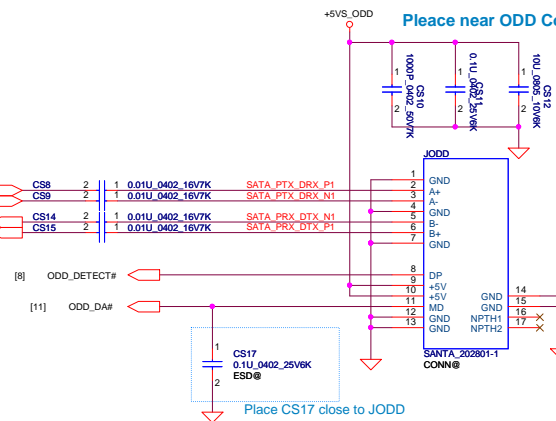


ODD Power Control



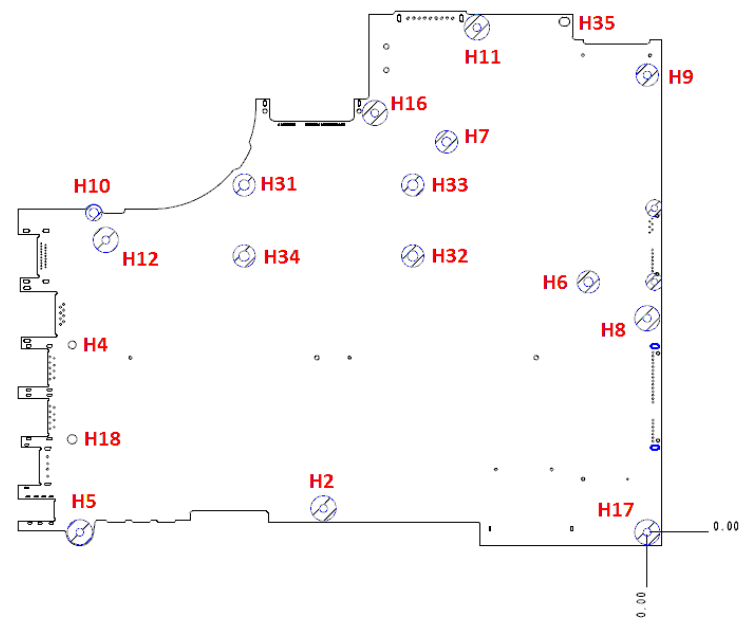
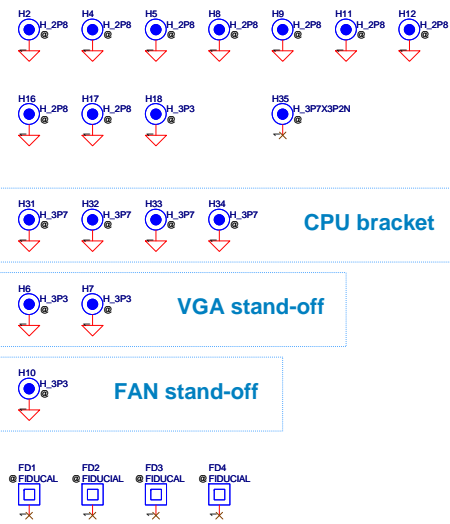
SATA ODD Connector

Place near ODD Connector



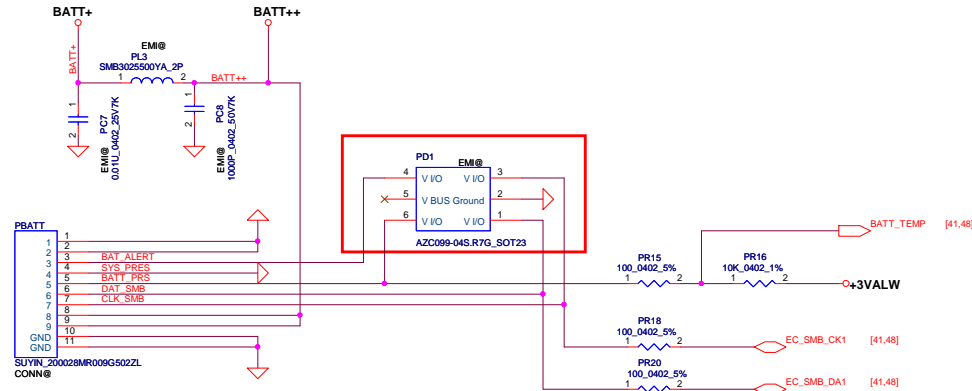
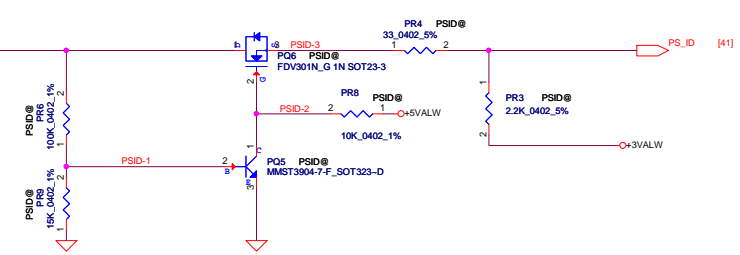
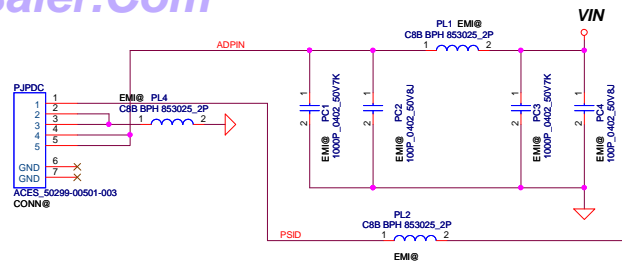
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2013/03/06		2014/04/01		Document Number	
				LA-A491P	
				Date: Thursday, May 23, 2013	
				Sheet 43 of 58	

Screw Hole

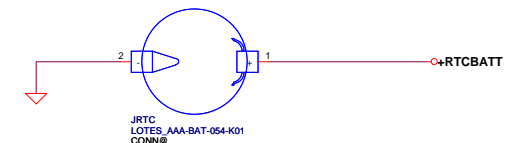


Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
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51							
52							
53							
54							



<p>ADP_I (with selector)</p>	<p>Adapter adaptor OC H_PROCHOT# 2ms while hybrid power transition</p>	<p>PH1 under CPU bottom side : CPU thermal protection at 93 +/- 3 degree C +EC_VCCA</p>
<p>Adapter protection: if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user</p>	<p>Battery protection: asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW_PROCHOT# is issued by EC</p>	<p>Erp lot6 Circuit</p>

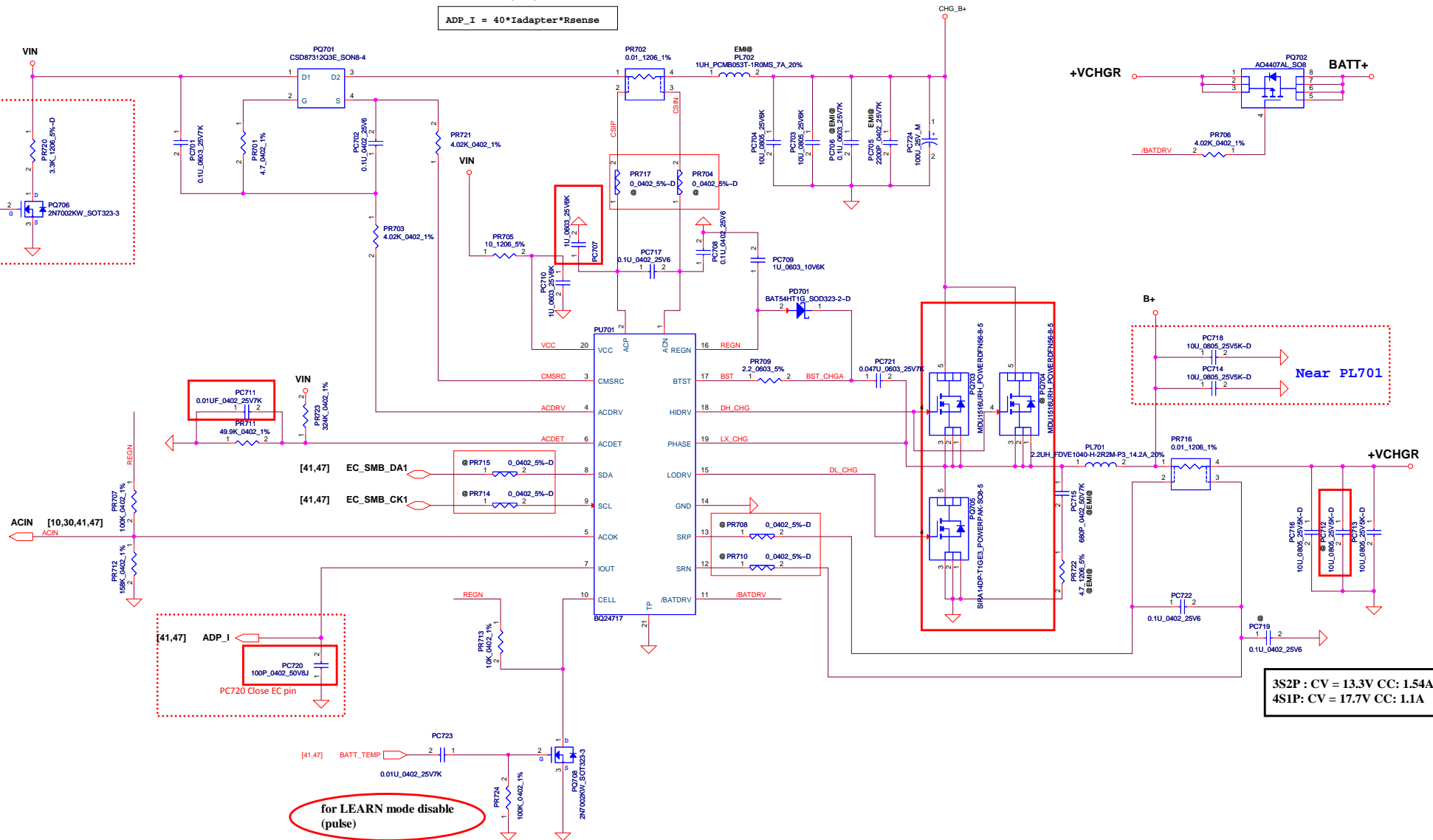


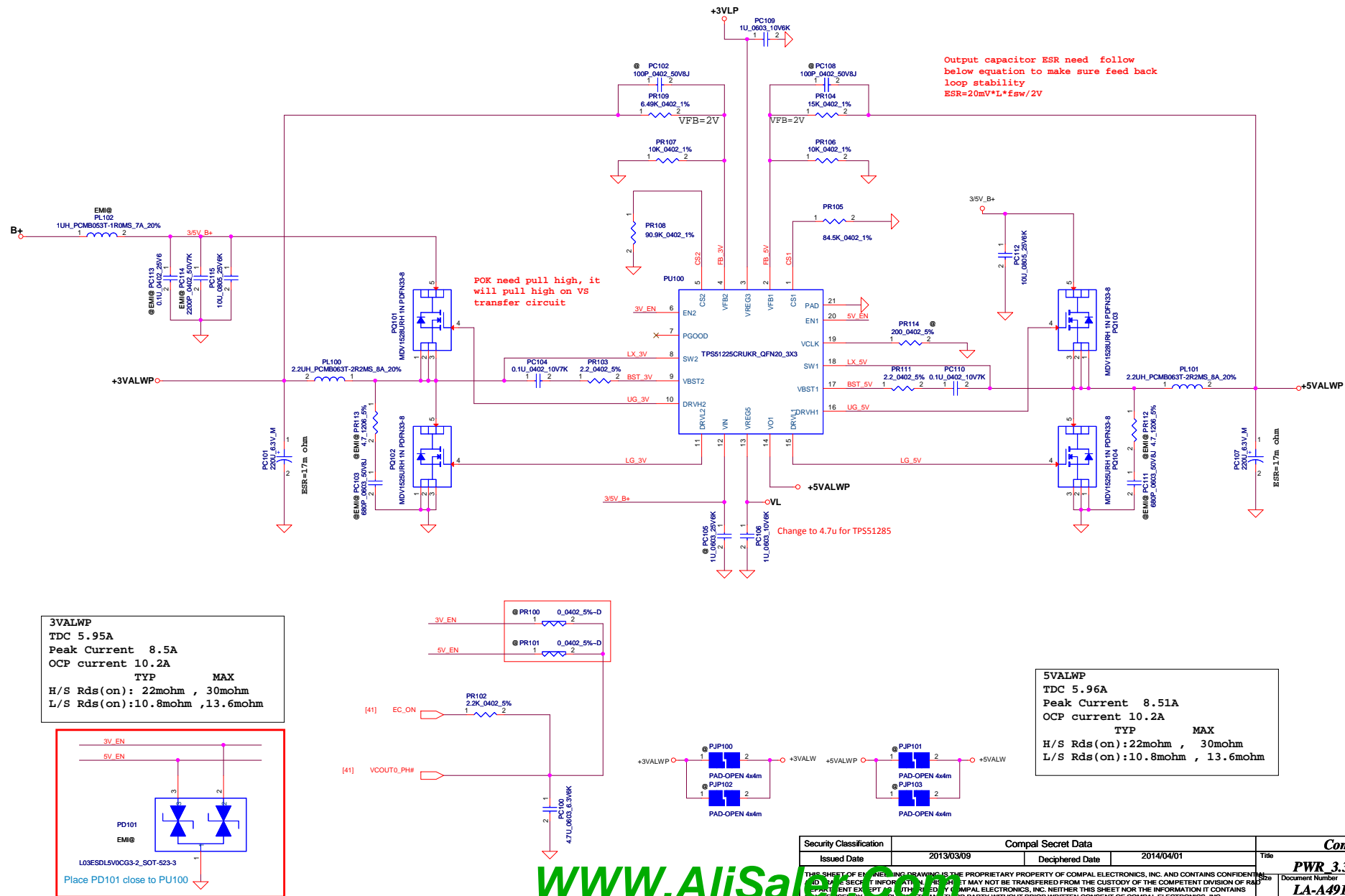
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	PWR DCIN/BATT CONN/OTP
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				LA-A491P	
Date:		Thursday, May 23, 2013		Sheet	47 of 58

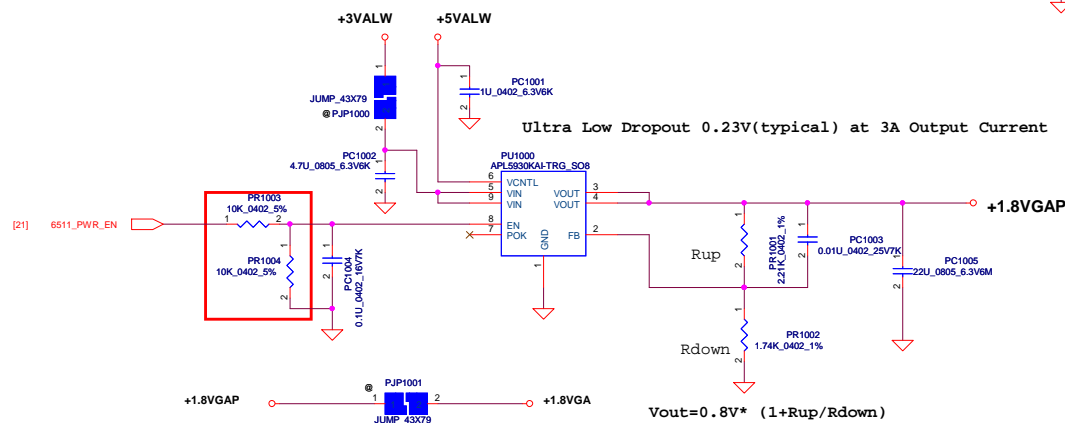
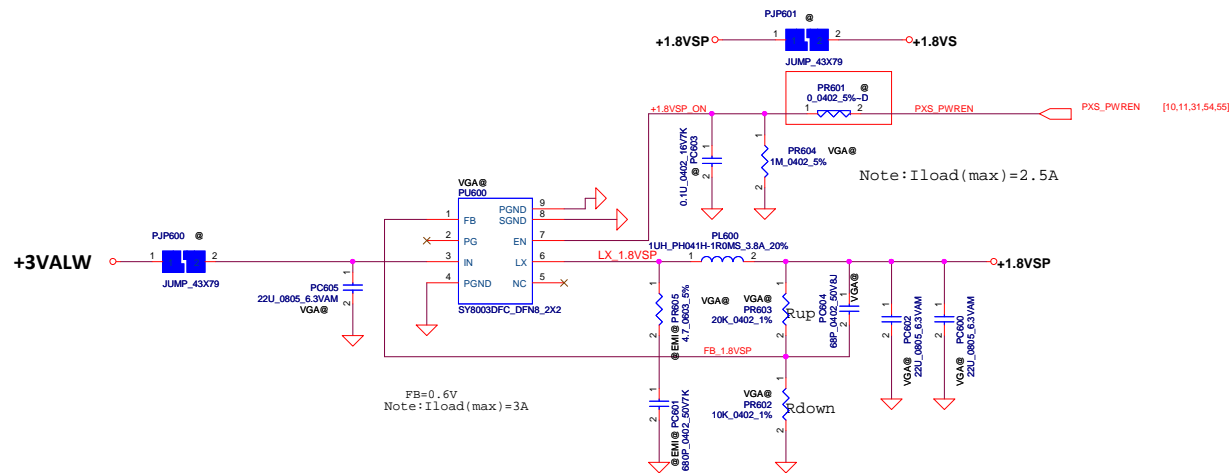
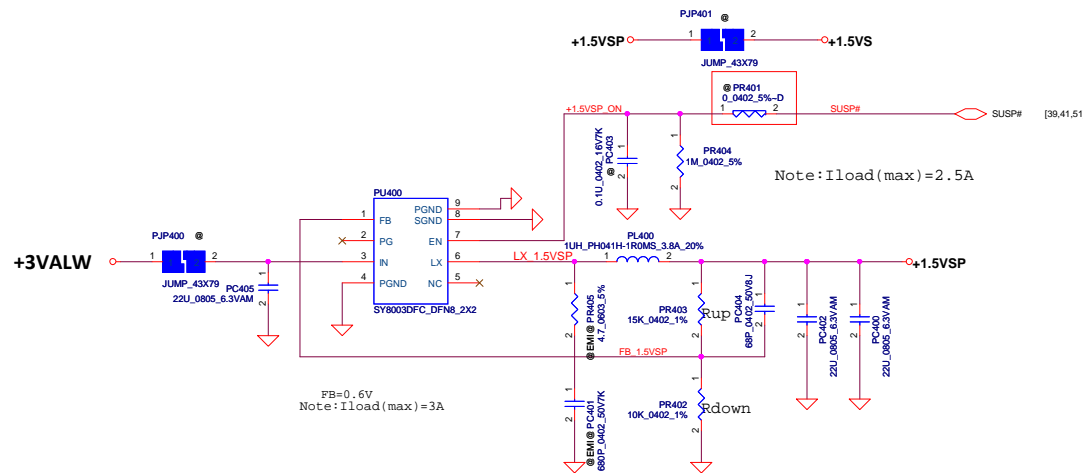
Iada=0~3.33A (65W)

Iada=0~4.62A (90W)

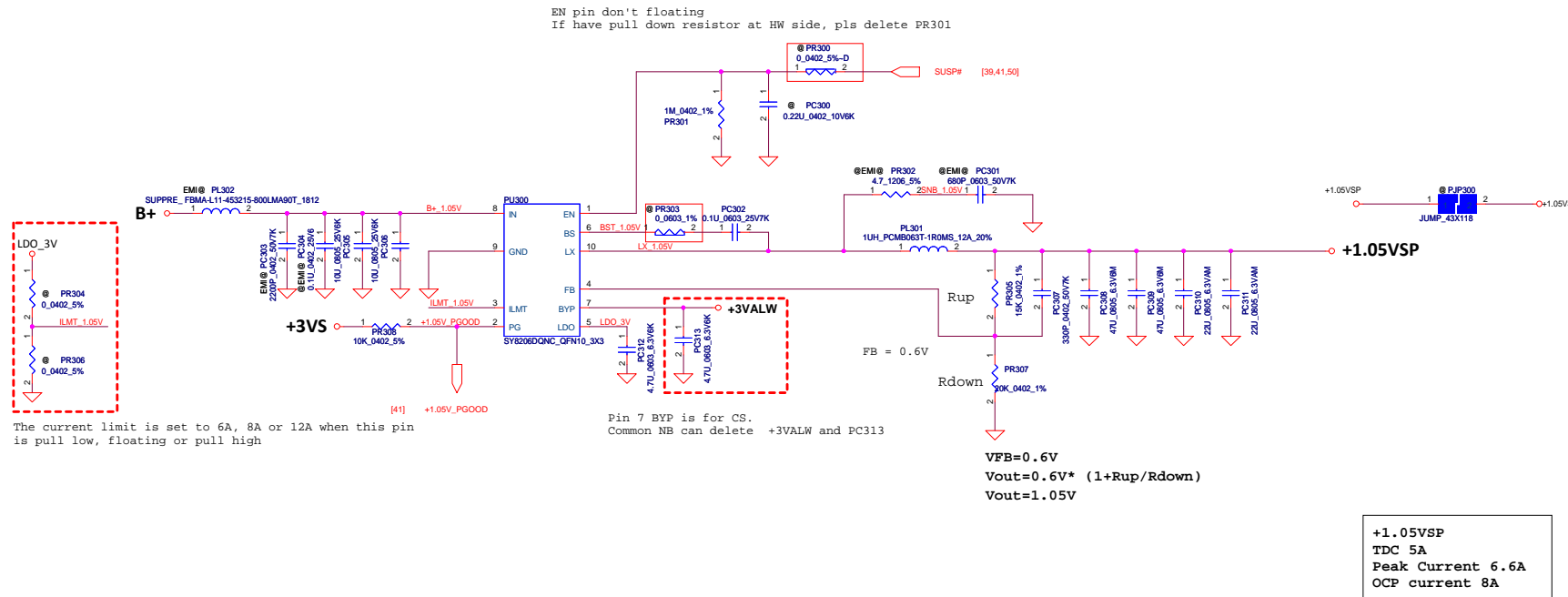
ADP_I = 40*Iadapter*Rsense

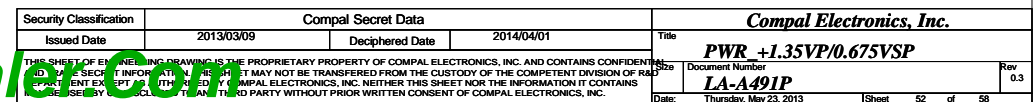


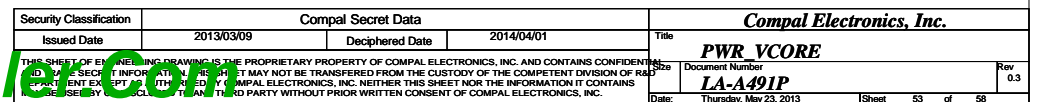




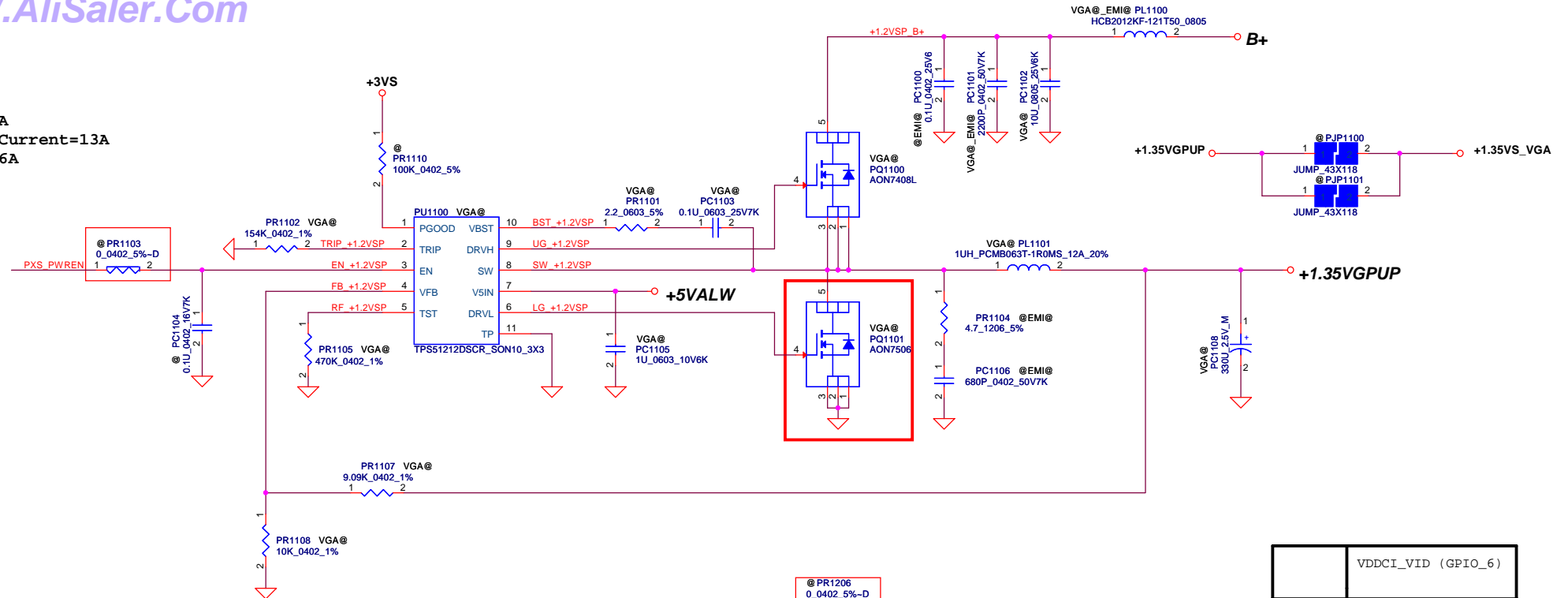
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	PWR 1.5VSP / 1.8VSP / 1.8VGAP	
Document Number		LA-A491P		Rev 0.3	
Date		Thursday, May 23, 2013		Sheet 50 of 58	



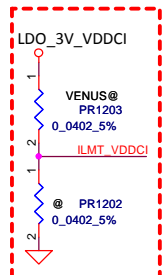




TDC=9A
Peak Current=13A
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V



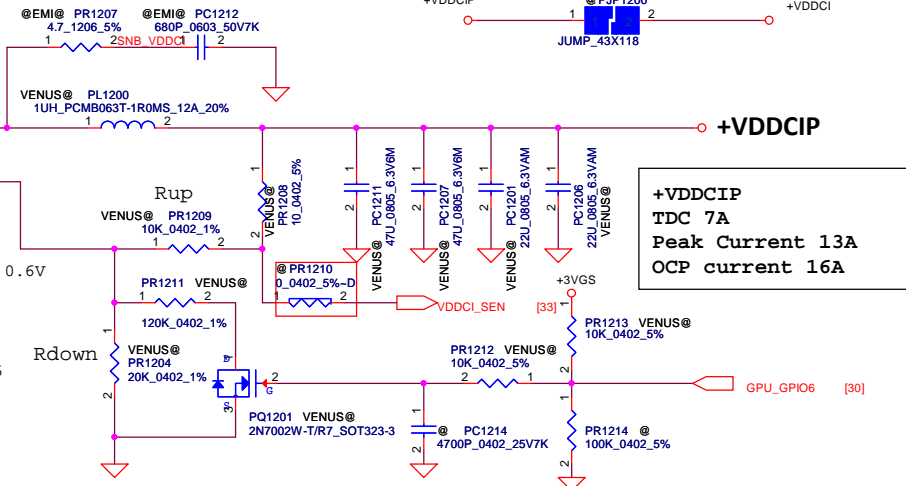
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

$$VFB=0.6V$$

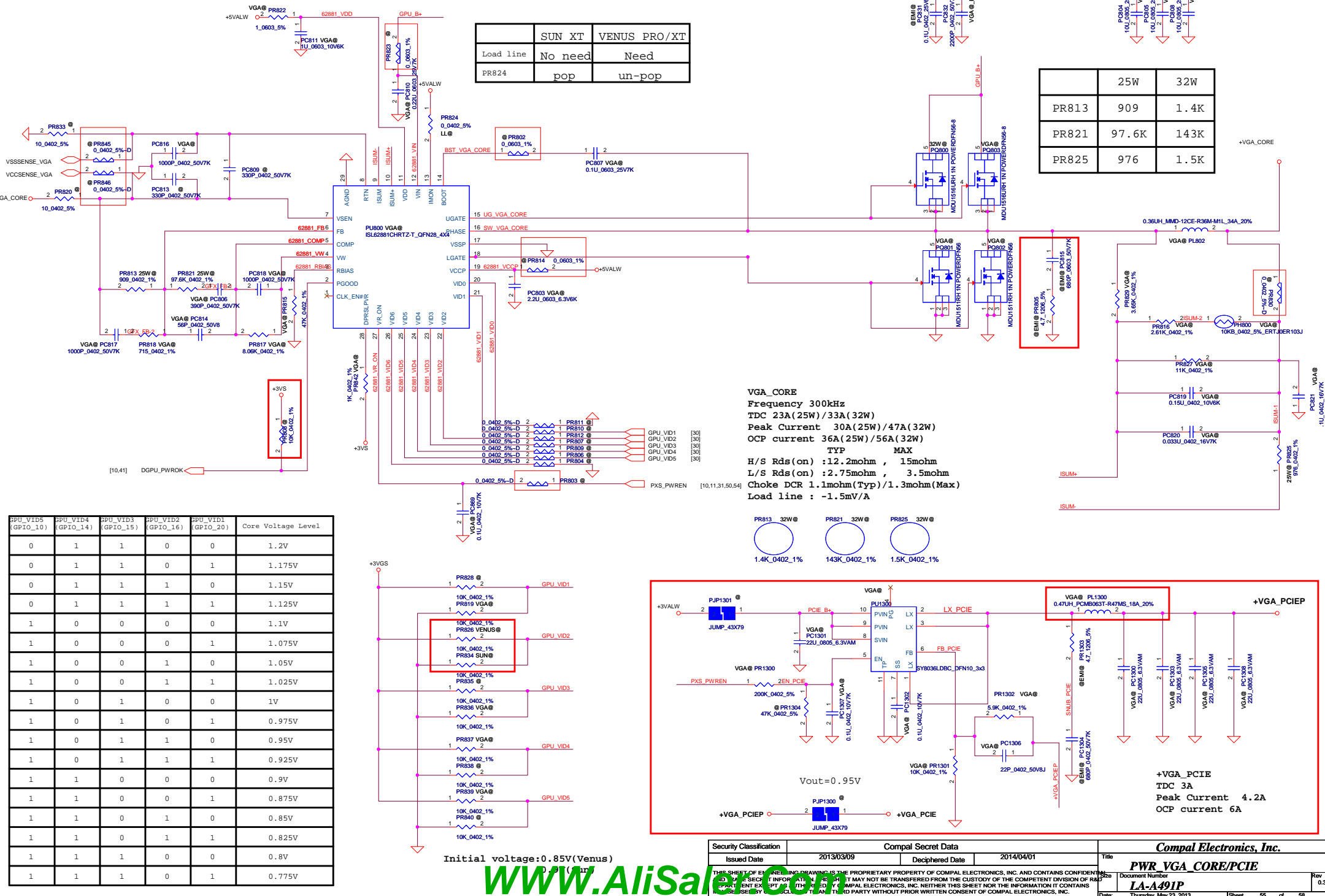
$$Vout=0.6V \cdot (1+Rup/Rdown)$$

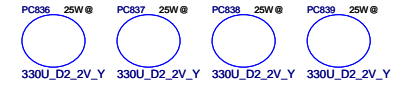
$$Vout=0.9V$$



+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A

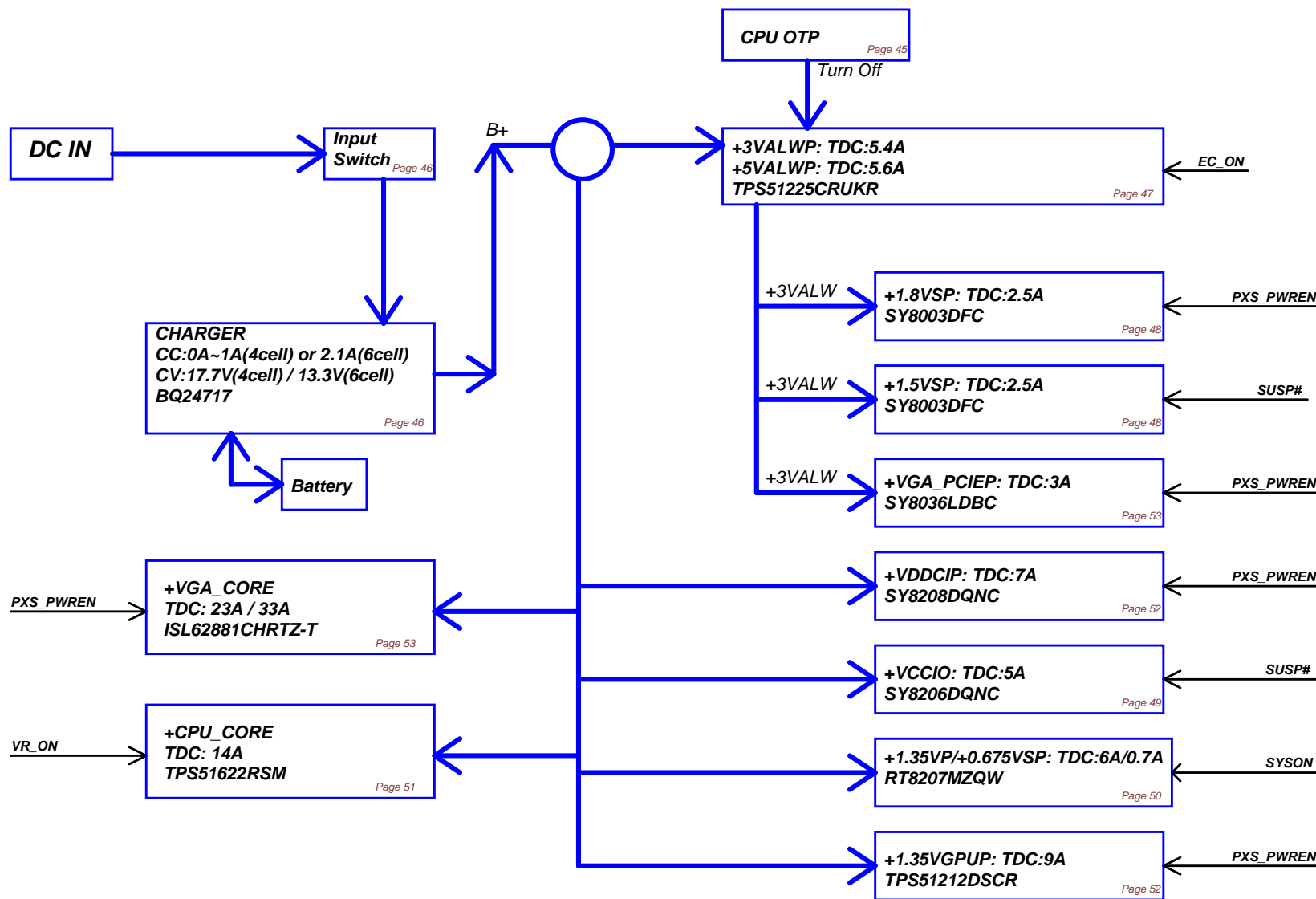
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Power block



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